



CST100N04 N-Ch 40V Fast Switching MOSFETs



- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

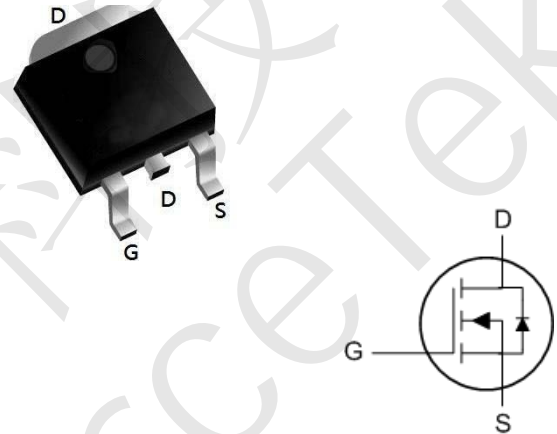
CST100N04 Product Summary

BVDSS	RDSON	ID
40V	3.8 mΩ	100A

CST100N04 Description

The CST100N04 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The CST100N04 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

CST100N04 TO252 Pin Configuration



CST100N04 Absolute Maximum Ratings (@ T_C = 25°C unless otherwise specified)

Symbol	Parameter	Value	Units
V _{DS}	Drain-to-Source Voltage	40	V
V _{GS}	Gate-to-Source Voltage	±20	V
I _D	Continuous Drain Current	T _C = 25°C	100
		T _C = 100°C	50
I _{DM}	Pulsed Drain Current ⁽¹⁾	320	A
E _{AS}	Single Pulsed Avalanche Energy ⁽²⁾	156	mJ
P _D	Power Dissipation	T _C = 25°C	142
R _{θJA}	Thermal Resistance, Junction to Ambient ⁽³⁾	31	°C/W
R _{θJC}	Thermal Resistance, Junction to Case	0.88	
T _J , T _{STG}	Junction & Storage Temperature Range	-55 to 150	°C



CST100N04 Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.3	1.9	2.5	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	-	3.8	4.9	m Ω
		$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$	-	5.7	7.4	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 20\text{V},$ $f = 1\text{MHz}$	-	3778	-	pF
C_{oss}	Output Capacitance		-	267	-	pF
C_{riss}	Reverse Transfer Capacitance		-	224	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 20\text{V}, I_D = 30\text{A}$	-	73	-	nC
Q_{gs}	Gate Source Charge		-	15	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	16	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 20\text{V}$ $I_D = 30\text{A}, R_{GEN} = 3\Omega$	-	12	-	ns
t_r	Turn-On Rise Time		-	29	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	60	-	ns
t_f	Turn-Off Fall Time		-	16	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	100	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	320	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 30\text{A}$	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	-	16	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	10	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 20\text{V}$, $V_G = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 0.5\text{mH}$, $I_{AS} = 25\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



CST100N04 Typical Performance

Figure 1: Output Characteristics

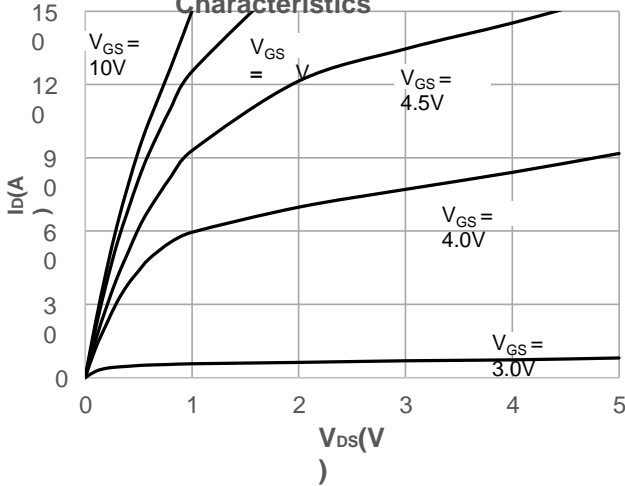


Figure 2: Typical Transfer Characteristics

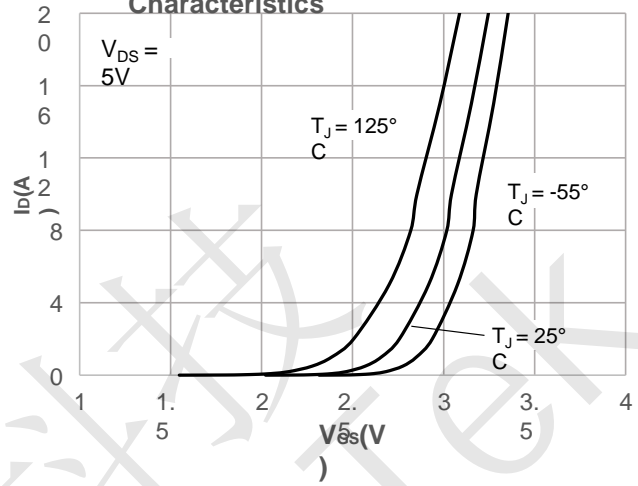


Figure 3: On-resistance vs. Drain Current

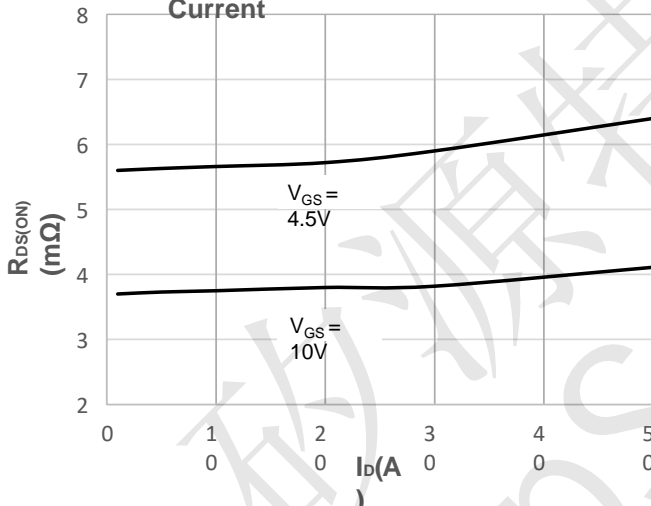


Figure 4: Body Diode Characteristics

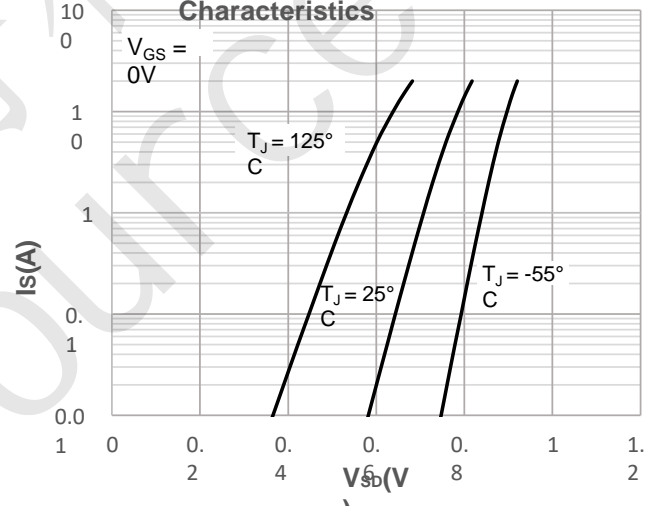


Figure 5: Gate Charge Characteristics

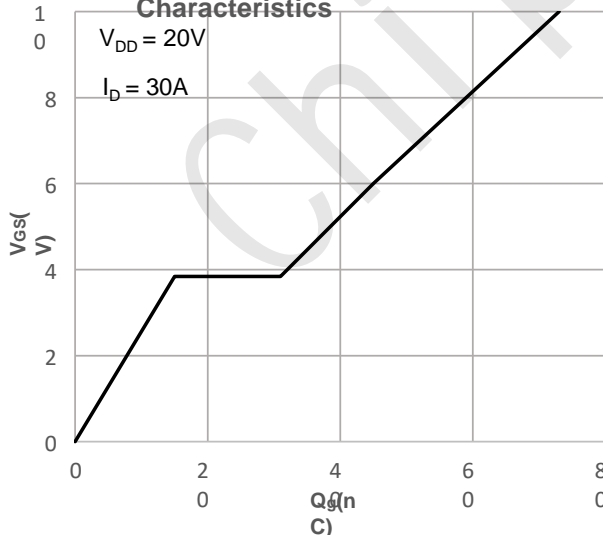
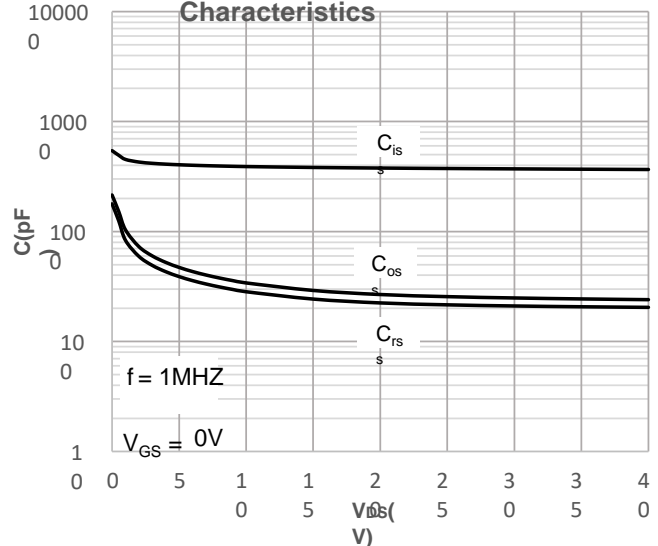


Figure 6: Capacitance Characteristics





CST100N04 Typical Performance

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

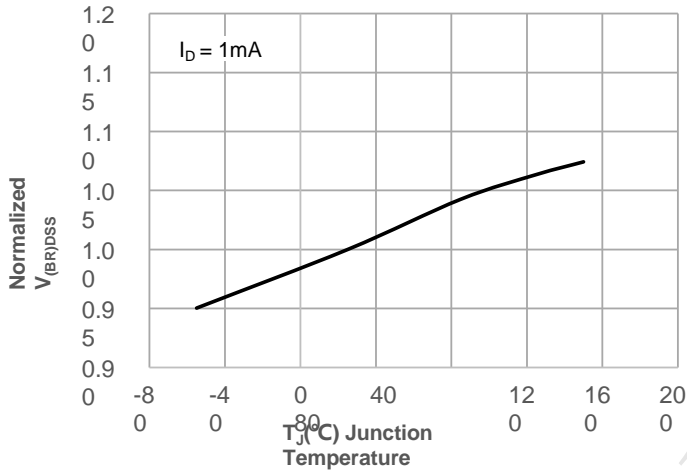


Figure 8: Normalized on Resistance vs. Junction Temperature

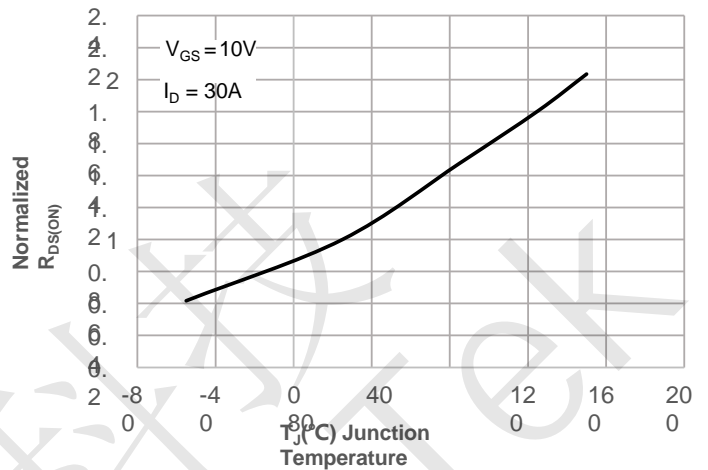


Figure 9: Maximum Safe Operating Area

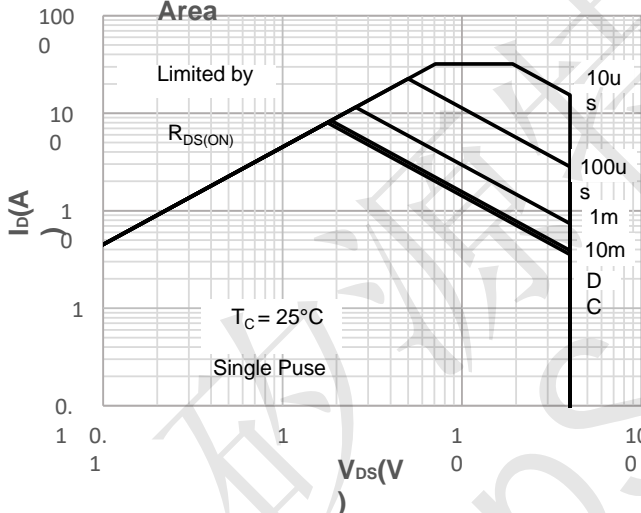


Figure 10: Maximum Continuous Drianc Current vs. Case Temperature

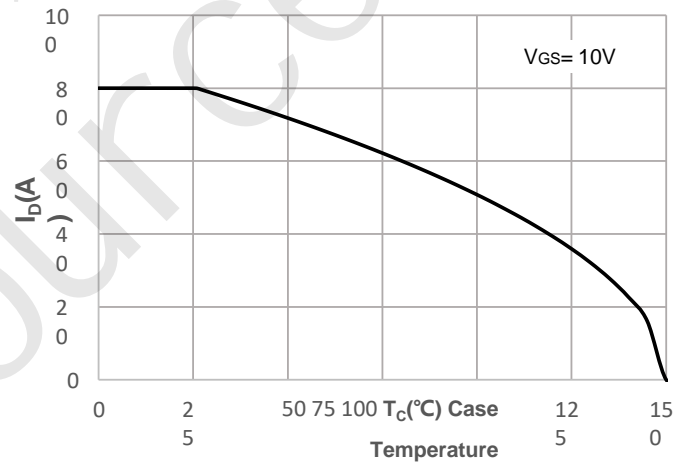


Figure 11: Normalized Maximum Transient Thermal Impedance

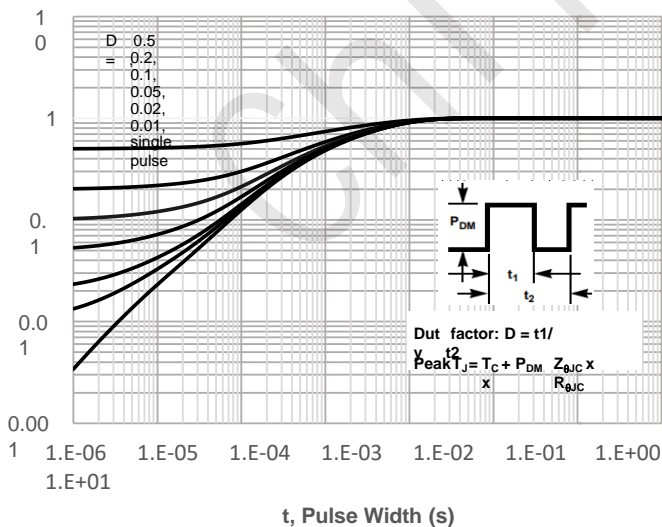
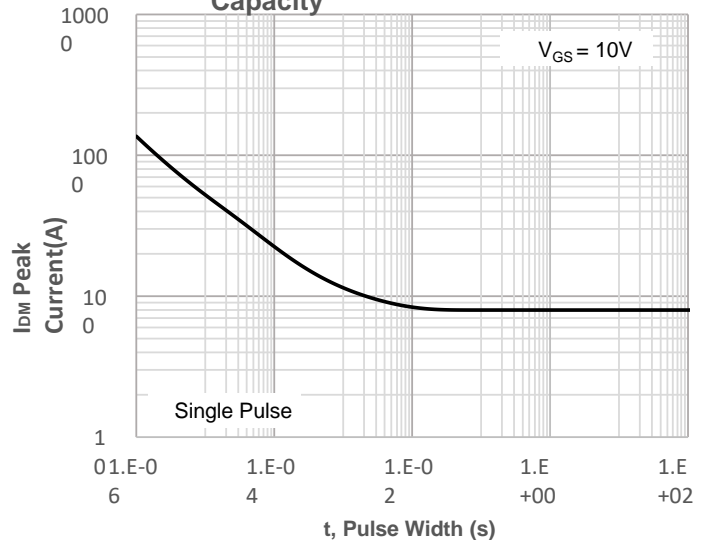


Figure 12: Peak Current Capacity





CST100N04 Test Circuit

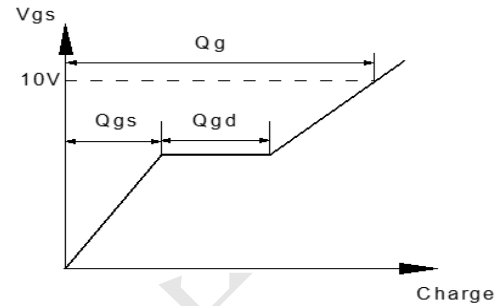
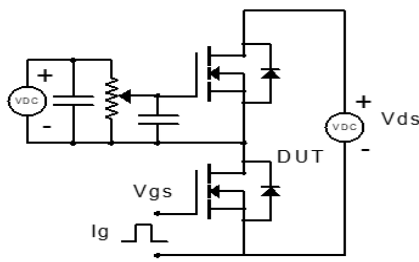


Figure 1: Gate Charge Test Circuit & Waveform

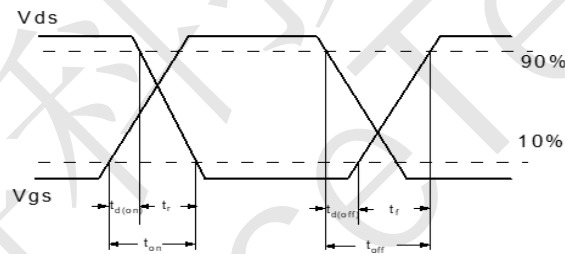
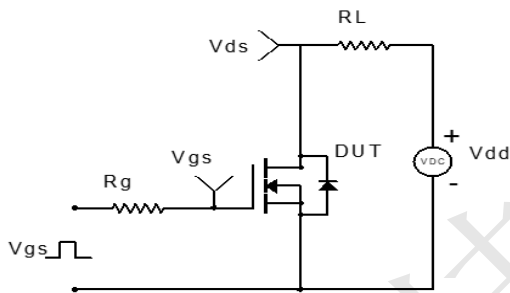


Figure 2: Resistive Switching Test Circuit & Waveform

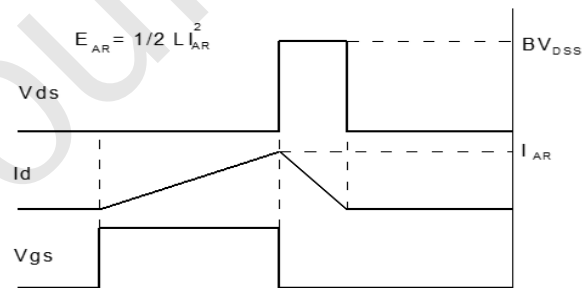
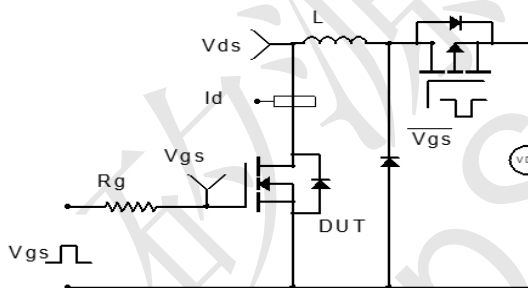


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

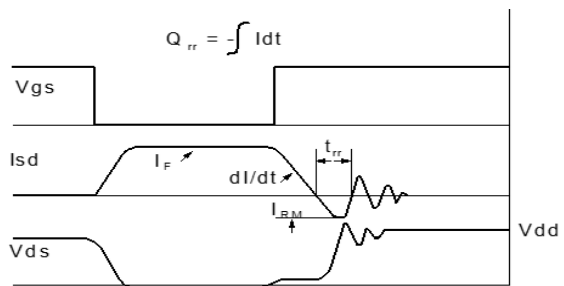
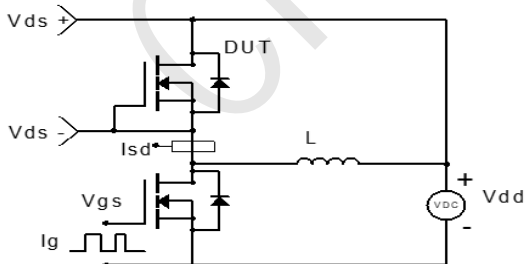
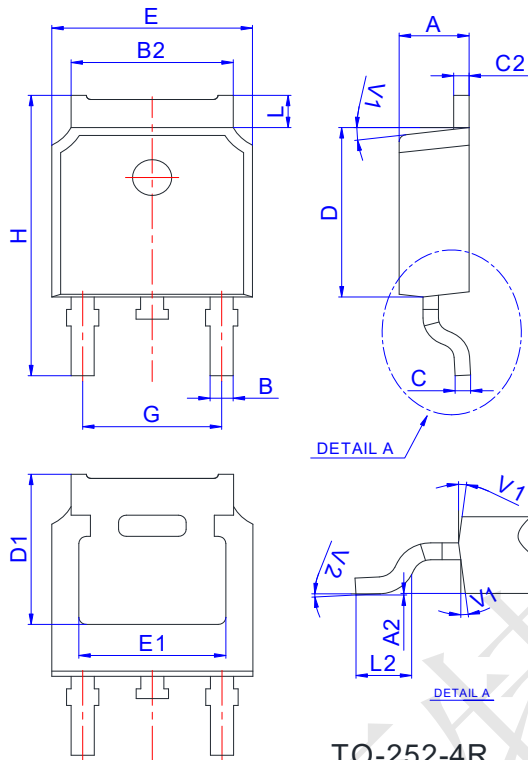


Figure 4: Diode Recovery Test Circuit & Waveform

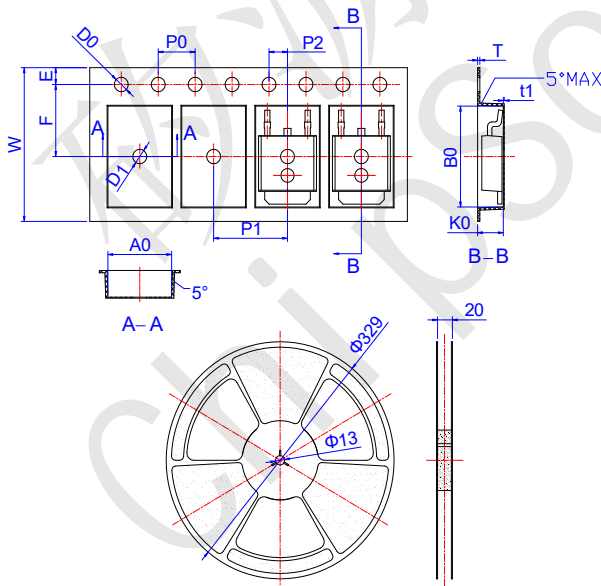


CST100N04 Package Mechanical Data-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

CST100N04 Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583