



CST4012 N-Ch and P-Ch Fast Switching MOSFETs

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

CST4012 Product Summary

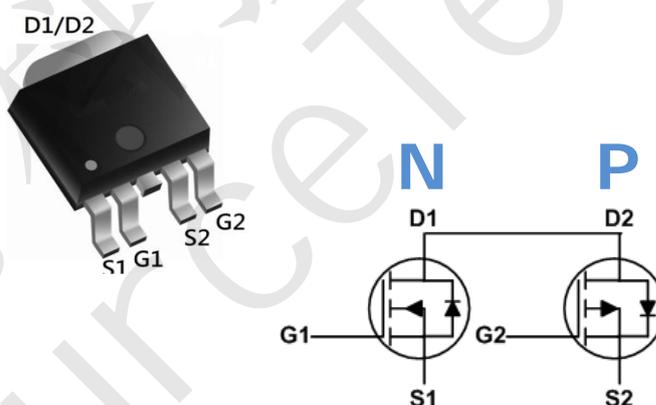


BVDSS	RDSON	ID
40V	17mΩ	25A
-40V	32mΩ	-25A

CST4012 Description

The CST4012 is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The CST4012 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

CST4012 TO252-4L Pin Configuration



CST4012 Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	25	-25	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	18	-16	A
I_{DM}	Pulsed Drain Current ²	46	-40	A
EAS	Single Pulse Avalanche Energy ³	28	66	mJ
I_{AS}	Avalanche Current	17.8	-27.2	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	25	31.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$

CST4012 Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	5	$^\circ C/W$



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CST4012 N-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=40V, V_{GS}=0V$	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=10V, I_D=8A$	-	17	22	m Ω
		$V_{GS}=4.5V, I_D=5A$	-	25	35	m Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V,$ $f=1.0MHz$	-	633	-	pF
C_{oss}	Output Capacitance		-	67	-	pF
C_{rss}	Reverse Transfer Capacitance		-	58	-	pF
Q_g	Total Gate Charge	$V_{DS}=20V, I_D=8A,$ $V_{GS}=10V$	-	12	-	nC
Q_{gs}	Gate-Source Charge		-	3.2	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	3.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=20V, R_L=2.5\Omega$ $V_{GS}=10V, R_{REN}=3\Omega$	-	4	-	ns
t_r	Turn-on Rise Time		-	3	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	15	-	ns
t_f	Turn-off Fall Time		-	2	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	32	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=8A$	-	-	1.2	V

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : $T_J=25^\circ\text{C}, V_{DD}=20V, V_G=10V, L=0.5mH, R_g=25\Omega, I_{AS}=7.2A$

$T_J=25^\circ\text{C}, V_{DD}=-20V, V_G=-10V, L=0.5mH, R_g=25\Omega, I_{AS}=-8.4A$

3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$



CST4012 N-Ch and P-Ch Fast Switching MOSFETs

CST4012 P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.012	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-8A$	---	32	45	m Ω
		$V_{GS}=-4.5V, I_D=-4A$	---	47	70	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.32	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-32V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-8A$	---	12.6	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	13	16	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-20V, V_{GS}=-4.5V, I_D=-12A$	---	9	---	nC
Q_{gs}	Gate-Source Charge		---	2.54	---	
Q_{gd}	Gate-Drain Charge		---	3.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-1A$	---	19.2	---	ns
T_r	Rise Time		---	12.8	---	
$T_{d(off)}$	Turn-Off Delay Time		---	48.6	---	
T_f	Fall Time		---	4.6	---	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	1004	---	pF
C_{oss}	Output Capacitance		---	108	---	
C_{rss}	Reverse Transfer Capacitance		---	80	---	

CST4012 Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	-20	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	-40	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1	V

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1\text{mH}, I_{AS}=-27.2A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.



CST4012 Typical Performance Characteristics-N

Figure 1: Output Characteristics

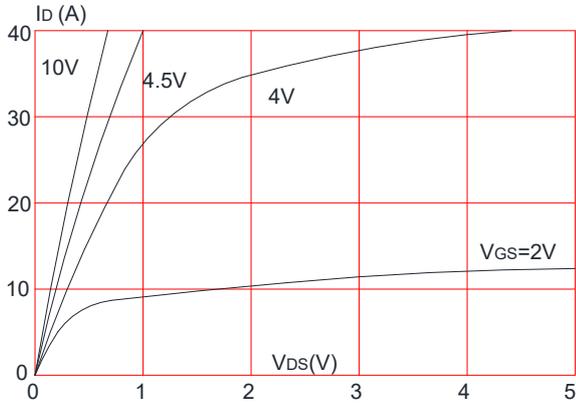


Figure 2: Typical Transfer Characteristics

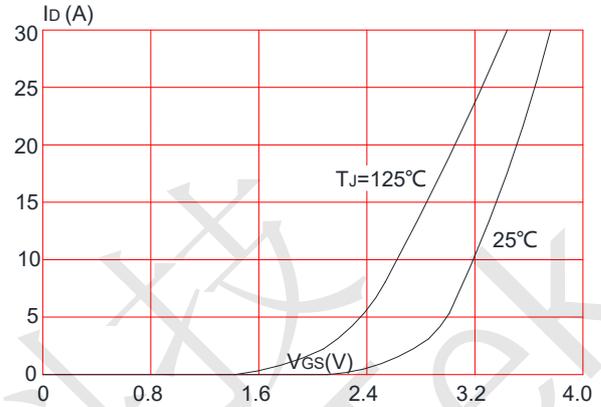


Figure 3: On-resistance vs. Drain Current

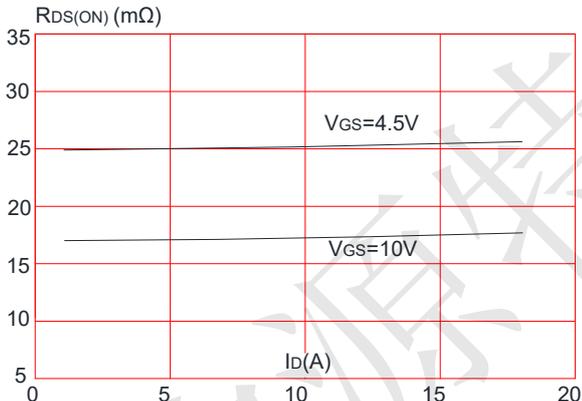


Figure 4: Body Diode Characteristics

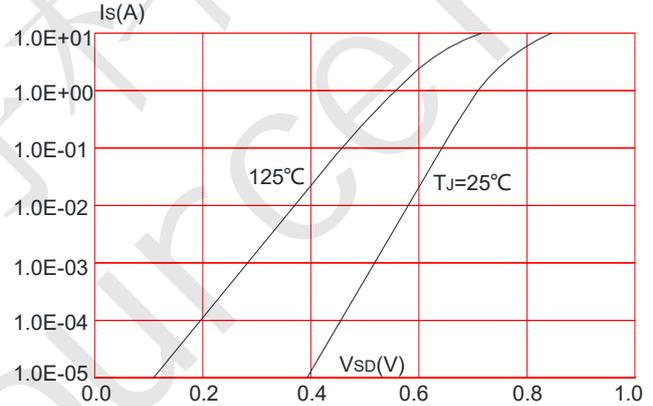


Figure 5: Gate Charge Characteristics

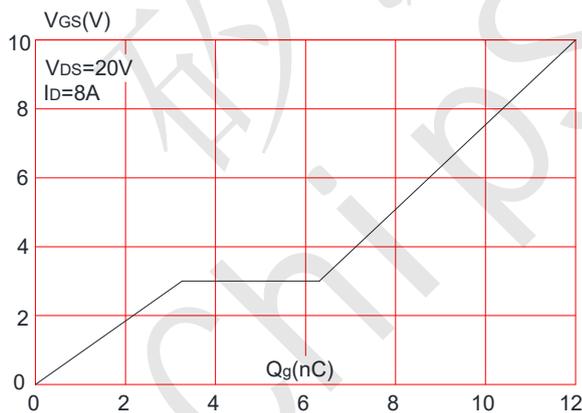
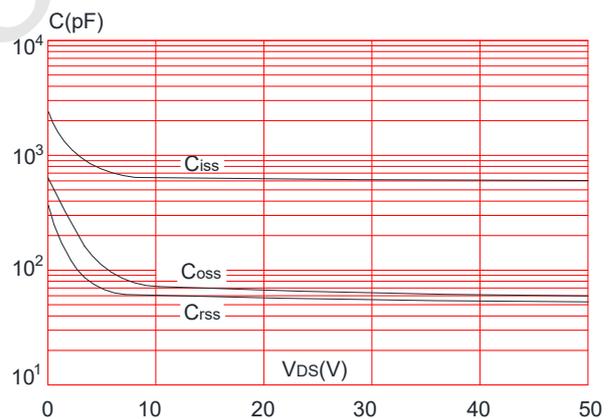


Figure 6: Capacitance Characteristics





CST4012 N-Ch and P-Ch Fast Switching MOSFETs

Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

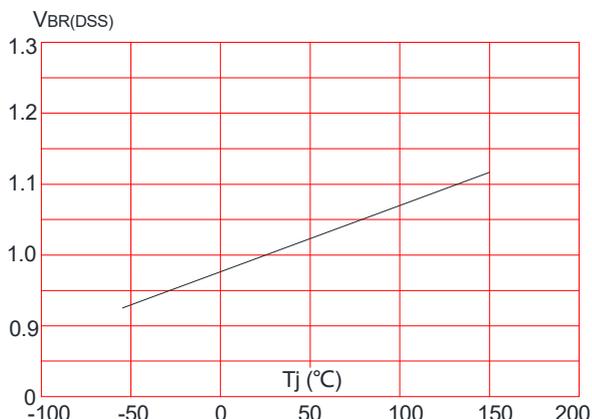


Figure 8: Normalized on Resistance vs. Junction Temperature

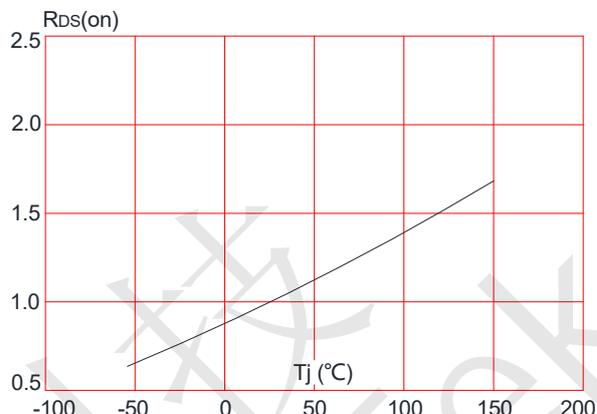


Figure 9: Maximum Safe Operating Area

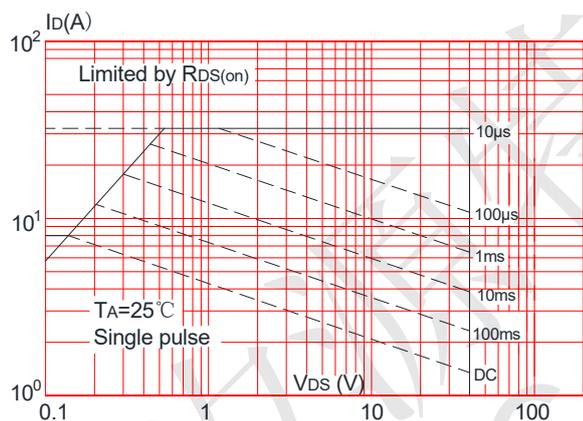


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

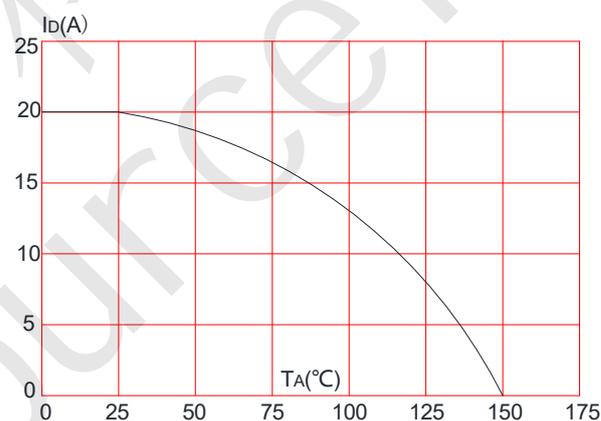
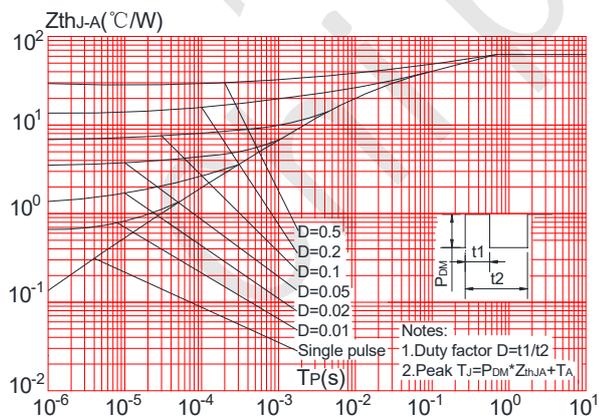


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient





CST4012 N-Ch and P-Ch Fast Switching MOSFETs

CST4012 P-Channel Typical Characteristics

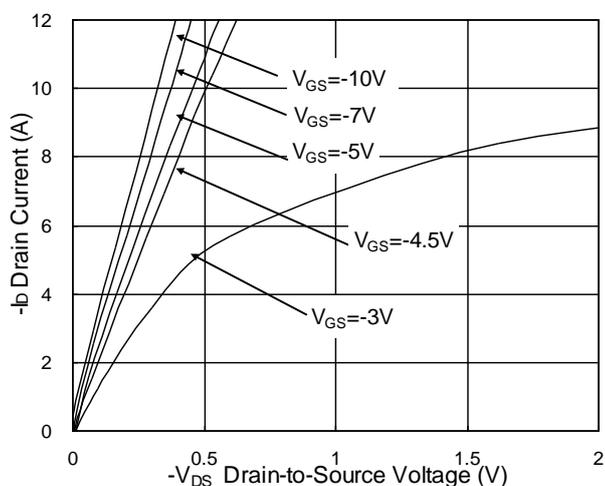


Fig.1 Typical Output Characteristics

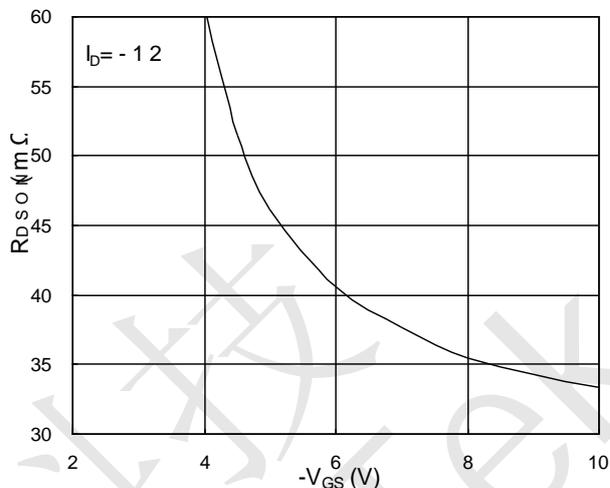


Fig.2 On-Resistance v.s Gate-Source

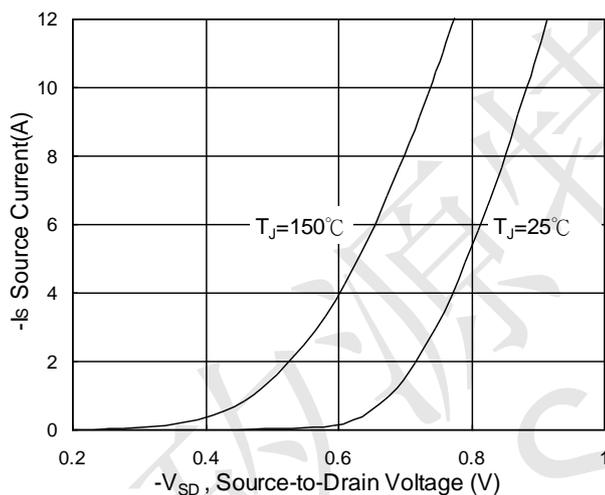


Fig.3 Forward Characteristics of Reverse

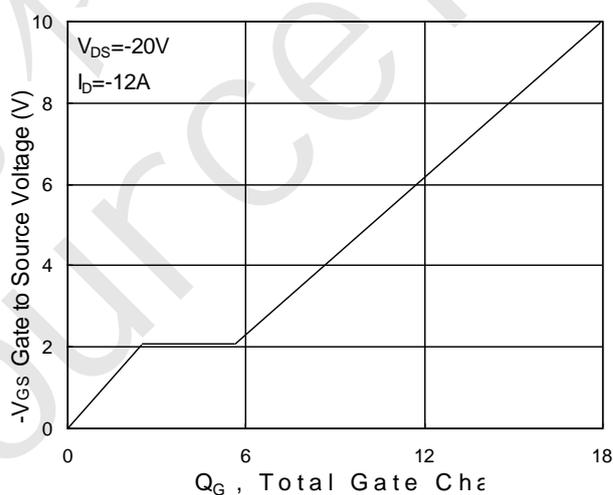


Fig.4 Gate-Charge Characteristics

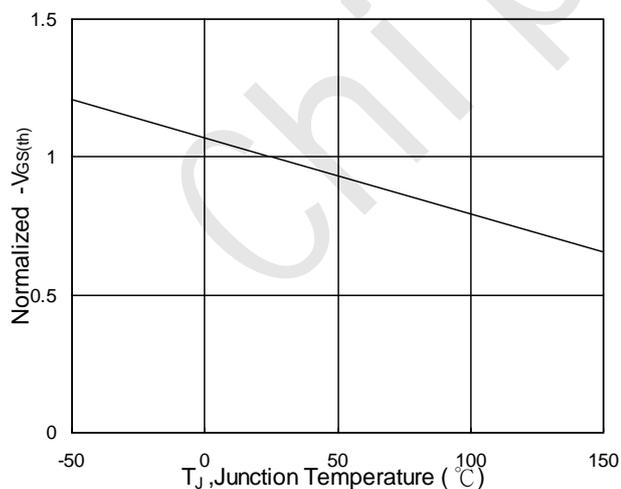


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

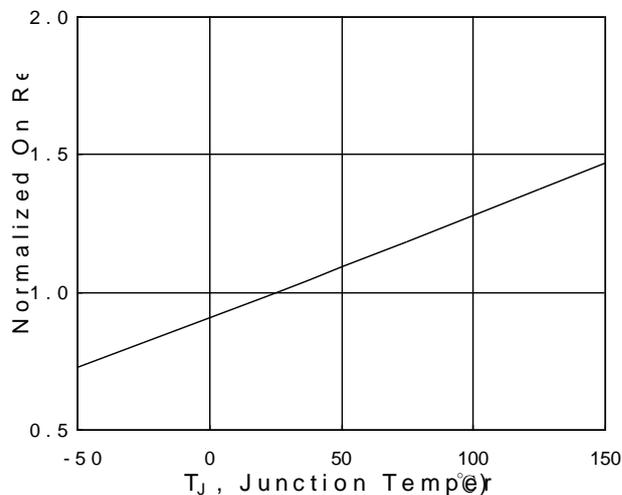


Fig.6 Normalized $R_{DS(on)}$ v.s T_J



CST4012 N-Ch and P-Ch Fast Switching MOSFETs

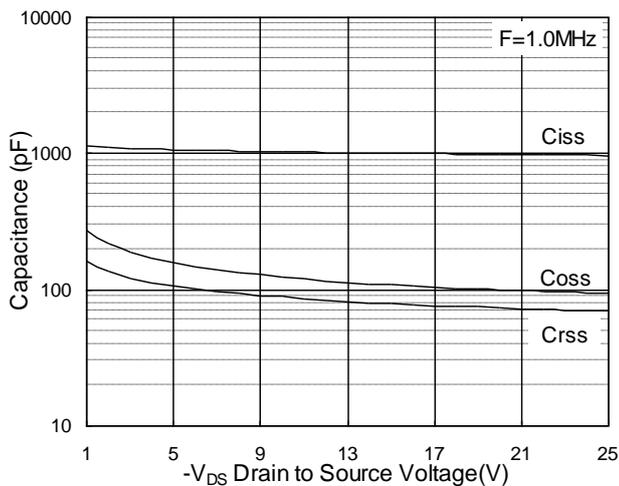


Fig.7 Capacitance

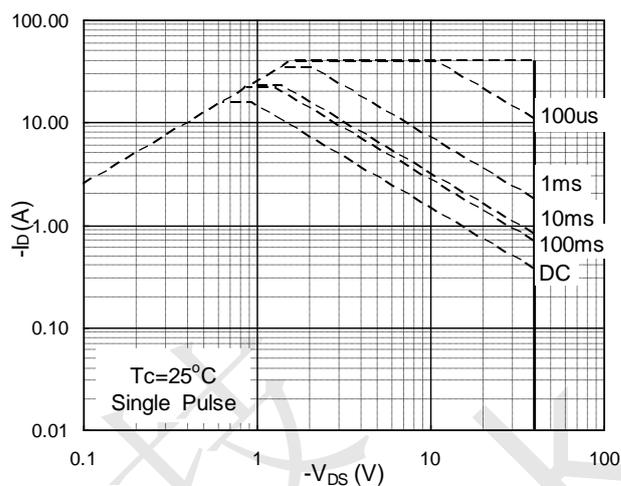


Fig.8 Safe Operating Area

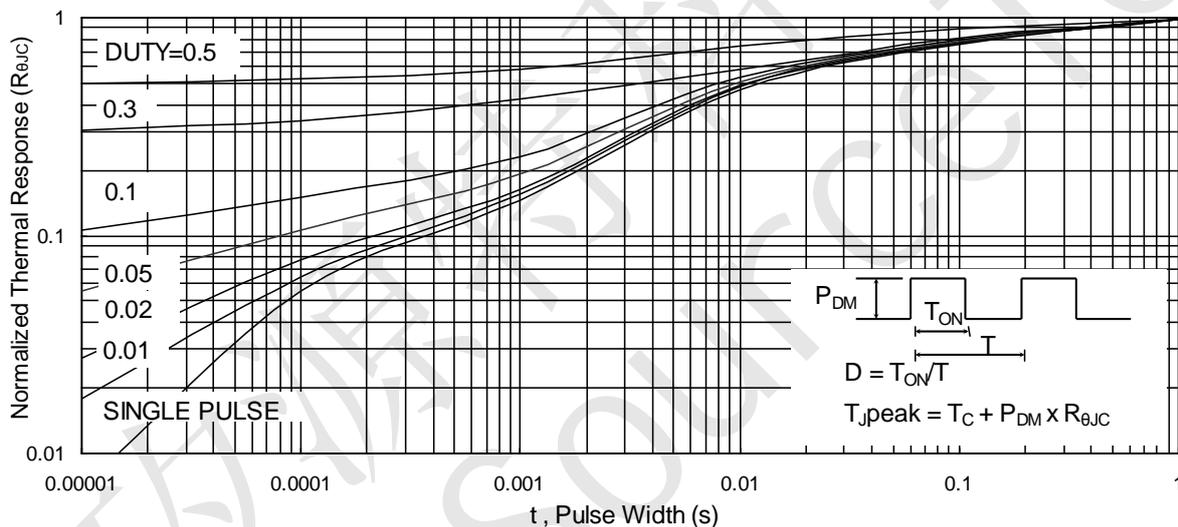


Fig.9 Normalized Maximum Transient Thermal Impedance

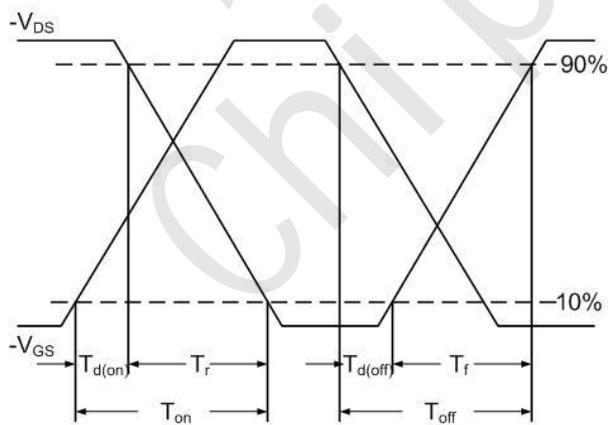


Fig.10 Switching Time Waveform

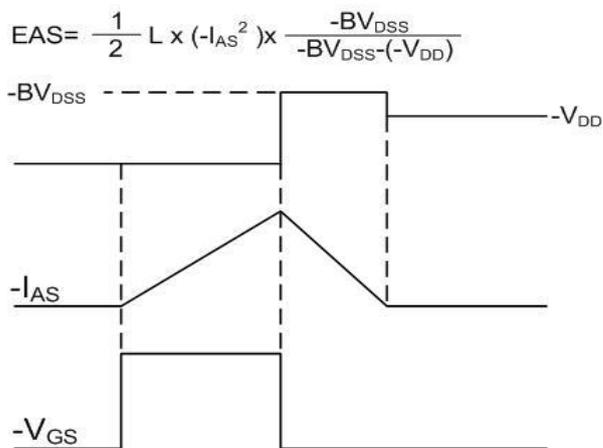


Fig.11 Unclamped Inductive Waveform

