TR16F032A(B)

Data Sheet

V1.8

32K Embedded Flash

Hi-Performance 16-bit Multimedia Processor

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

1. TR16F032A/B General Description

The **TxP16E**™ is a high performance 16-bit MCU, running up to 32MHz and provided with 32K FLASH and total 4K SRAM for high performance process of audio algorithm, power control and motor control. It is the new generation computational kernel for Flash DSP series. It has initially aimed at the areas of controller and multimedia digital signal processing (DSP) application to demonstrate its profession. TxP16E furnish with fast **MAC** architecture, which allows multiplication+accumulation instructions to be issued with access memory simultaneously during one cycles. The TR16F032 is equipped with TxP16E and integrating input/output ports, Audio PWM, Timer and Low Voltage Reset...etc on a chip. Built-in high-speed 10-bit ADC can apply to AC power and motor control application easily.

Furthermore, TR16F032 extend its external device connection capability such as Serial ROM/Flash. The internal memory capacity includes 32Kx16 program/data FLASH plus 4Kx16 working SRAM.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

2. TR16F032A/B Features

- High-performance RISC TxP16E CPU
  - wide working frequency and voltage 1Mhz ~32Mhz@1.8Volt ~ 5.5Volt
  - Operation frequency is programmable by Software
  - Built-in 4096x16 SRAM
  - Hybrid Instruction and data memory share with 32Kx16 Flash ROM
  - Embedded PC Stack Level 24
- Rich DSP function
  - Hardware Circular Buffer support
  - MAC Computation power : 32MIPS (max.)
  - Multi-Function Support: In MAC calculation, simultaneously access two operands from memory in one cycle
  - Extend Dynamic Range: A 40-bit accumulator to ensure in 512 successive multiple+additions no overflows
- Embedded Flash 32Kx16
  - Typical 100,000(TR16F032A) / 20,000(TR16F032B) erase/program cycles
  - Greater than 10 years Data Retention
- Software-based audio processing technical
  - Subband, ADPCM , CELP , Melody systhesis up to 20 channels (Max)
- Support 20+2(ICE PAD can be as I/O) general purpose I/O port, can be configured to open-drain output
- Stereo 8~ 16-bit PWM can be adjustable
- 15 IRQ & 1 NMI
  - NMI is non-mask interrupt, can interrupt IRQ immediately
  - 2 external interrupt
- 4 bit SPI Master Hardware support DMA transfer
- SPI Slaver
- Green Mode
- Timer1 , Timer2 with Pre-scale
- Low power instruction
- 24-Hours / One day Real-Time Clock
- ICE support Data RAM monitor for motor control debug
- Support Spread Spectrum clocking to reduce EMI.
- CPU Array
- Watch dog timer (WDT)
- Low voltage reset (LVR)
- Low dropout regulator(LDO) supply 3.3V/1.8V@20mA (voltage drop 0.1v)
- PB0, PB1, PB2, PB3 support two edge modes for wake-up function are rising and falling edge trigger.
- Comparators
- ADC 10bit / 285 kbps(@ACQT = 4*TAD) / 8 channel

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

- Temp. Sensor
- Microphone
- 1402 interface
- ***New instruction about ACALL, please refer to "TxP16E Instruction Set Reference"***
- ***New instruction about 3OP, please refer to "TxP16E Instruction Set Reference"***
- ***New instruction about Barrel Shifter, please refer to "TxP16E Instruction Set Reference"***
- ***New instruction about Immediate Value CBL, please refer to "TxP16E Instruction Set Reference"***
- ***Notice item about Flash DSP programming, please refer to "Flash DSP Programming Note(AN0060)"***

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

3. TR16F032A/B Application Field

- MCU Application
- Electronic Dictionary
- Handheld Games
- Electronic Learning Aid (ELA)
- Digital Photo Frame
- Electronics storybook
- Power / motor control

4. TR16F032A/B Block Diagram

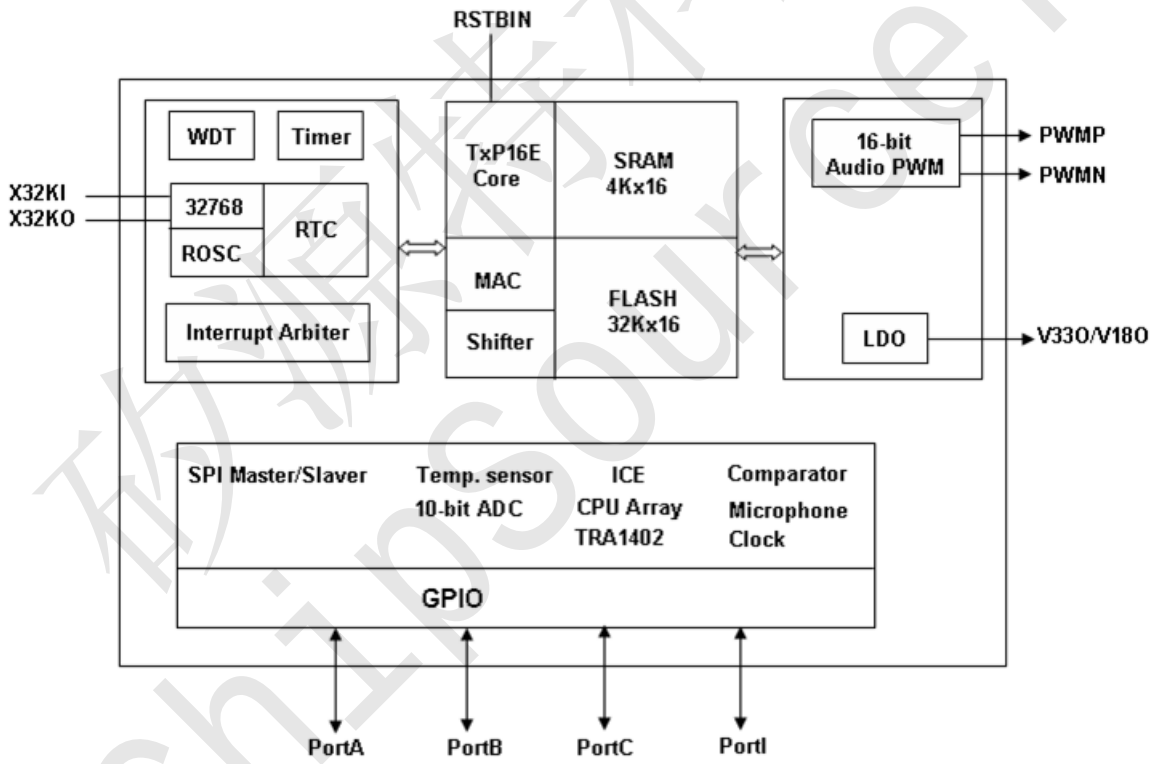


Figure 4.1

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

4.1 Pin Assignments /Description

Pin Name	I/O	State after RESET	FUNCTIONS
Chip Power			
VCC	I	High	Chip Power Input
VSS	I	Low	Digital Ground
AVSS	I	Low	Analog Ground
VIO	I	High	PortA IO Power input
V33O	O	High	3.3V/1.8V LDO Power Output
VPD	I	High	PWM IO PAD Power Input
VPS	I	Low	PWM IO PAD Ground
Chip Control			
RSTINB	I	High	Low force chip to enter reset mode, internal 30K ohm pull-up
General Purpose I/O Port			
PortA[5:0]	I/O	Low	PortA is programmable Input/Output port
PortB[5:0]	I/O	Low	PortB is programmable Input/Output port
PortC[7:2]	I/O	Low	PortC[7:2] is programmable Input/Output port
PortC[1]/ X32KI	I/O	Low	PortC[1] is programmable Input/Output port X32KI: 32K crystal input
PortC[0]/ X32KO	I/O	Low	PortC[0] is programmable Input/Output port X32KO: 32K crystal output
PortI[1]/ ICE_SCLK	I/O	Low	PortI[1] is programmable Input/Output port ICE_SCLK: embedded ICE clock pin
PortI[0]/ ICE_SD	I/O	Low	PortI[0] is programmable Input/Output port ICE_SD: embedded ICE data pin
PWM Audio			
PWMP	O	Low	Digital PWM output(+)
PWMN	O	Low	Digital PWM output(-)

Notice:

1. VPD VPS Decoupling Cap 47uF, please close to IC nearly.

2. Power Path of VPD and VPS must pass through Decoupling Cap 47uF into IC.

3. VCC VSS Decoupling Cap 0.1uF, please close to IC nearly.

4. Power Path of VCC and VSS must pass through Decoupling Cap 0.1uF into IC.

5. VSS and AVSS are as close as possible.

6. PCB Layout about power line, Please refer to "Application Note(AN0059)"

7. It should be avoided that INTENA bit0 is turned on/off quickly. If need to turned on/off INTENA bit0 quickly, recommend to use INTMASK bit0. About detail, please refer to "FDSP programming guide".

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5. TR16F032A/B Function Descriptions

5.1 TxP16E

As shown in the block diagram in Figure 4.1, the TxP16E with MAC module is a 16-bit data width processing capability and all instructions are operated in one cycle except parameter data ROM(PM) access. The TxP16E not only provides general arithmetic such as addition, subtraction, shifter, normalize, and other logical operations, but it also involves MAC and circular buffer operations for complexity digital signal processing.

5.2 TxP16E Registers

The TxP16E contains of register files are illustrated below:

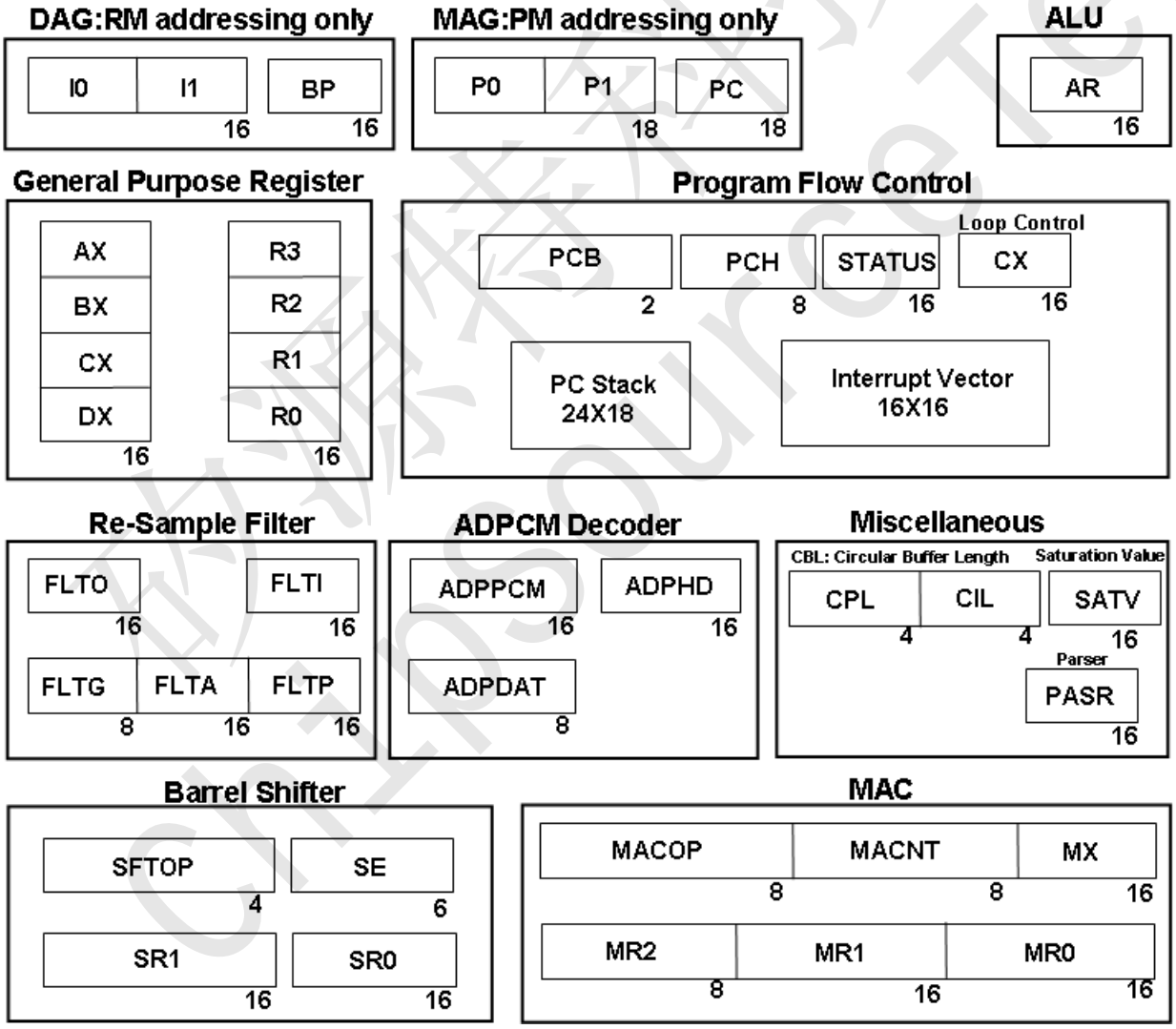


Figure 5.1 TxP16E Processor Core Registers

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

■ REGISTER FILES DEFINE:

AR: Accumulator Register
I0: Index 0 Register
I1: Index 1 Register
BP: Base Pointer Register
P0: Pointer 0 Register
P1: Pointer 1 Register
MACOP: MAC Operation Register
MACNT: MAC Operation Loop Counter
MX: MUL/MAC Input X Register
MR0: MUL/MAC Result Register 0
MR1: MUL/MAC Result Register 1
SFTOP: Shifter Operation Register
SE: Shifter Exponent Register
MR2: MUL/MAC Result Register 2
AX: General AX Register
BX: General BX Register
CX: General CX Register
DX: General DX Register
R0: General R0 Register
R1: General R1 Register
R2: General R2 Register
R3: General R3 Register
CBL: Circular Buffer Length Register
PASR: Parser Register
SR1: Shifter Result Register 1
SR0: Shifter Result Register 0

5.2.1 Special Registers

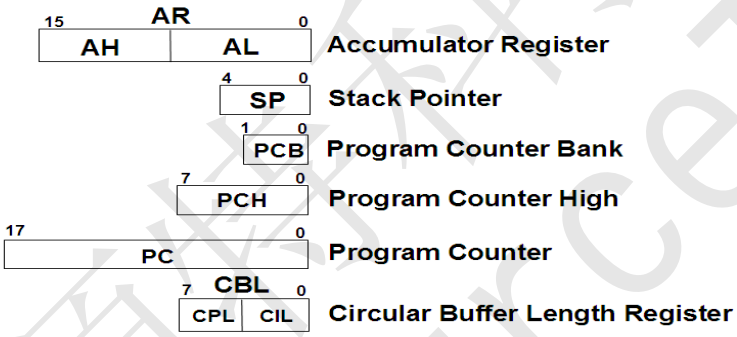


Figure 5.2 TxP16E Special Registers

- Accumulator Register

The AR is a general-purpose 16-bit register that stores the result of last arithmetic or logical operation. In addition, any data write to AR will affect the status flag.

- Stack Pointer

The SP is a 5-bit register that is for addressing Stack position. The SP will automatically increment / decrement cause by instruction “CALL” / “RETS”, and more detail revealed as the “PC Stack” section.

- Program Counter Bank

The program memory map is divided into 4 banks by PCB register (Program Counter Bank). Both BANK1 and BANK3 are system reserved. The BANK0 and BANK2 are implemented as Flash memory and static RAM, respectively.

- Program Counter High

The instruction “LJMP” and “LCALL” will refer PCH and PCB registers to compose of 18-bit pointer provides the 4x64K words PM addressing range.

- Program Counter

The 18-bit PC register provides 4x64K-word addressing capability. It is responsible for MCU fetch now executing instruction.

- Circular Buffer Length Register

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Many algorithms such as convolution, correlation, and digital filter require the circular data buffers. The TxP16E supports circular buffer operating via the I0 vs. CIL and P0 vs. CPL. The modulus logic implements automatic modulus addressing for accessing RM/PM circular buffer data.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.2.2 Common I/O Registers

The TxP16E involves 32 common I/O registers are shown in Table 5.1. There are defined the peripheral IO control and system register.

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	20	R/W	INTEN	OSC_EN	-	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	0	IntPrWR	0	SPIS_EN	SPIM_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	
IntVect	03H	XX	R/W	IntVect[15:0]								Interrupt Vector access Window
IOC_PA	04H	00	R/W	IOC_PA[5:0]								“1”= out, “0” = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[5:0]								“1”= out, “0” = in of related PB bit
IOC_PCI.L	06H	00	R/W	IOC_PC[7:0]								“1”= out, “0” = in of related PC bit
IOC_PCI.H	06H	00	R/W	IOC_PI[1:0]								1”= out, “0” = in of related PI bit
PortA	07H	XX	R/W	PortA[5:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[5:0]								Read: in port Write: out port
PortCI.L	09H	XX	R/W	PortC[7:0]								Read: in port Write: out port
PortCI.H	09H	XX	R/W	PortI[1:0]								Read: in port Write: out port
INTMASK.L	0AH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0AH	00	R/W	0	Mask14	Mask13	Mask12	Mask11	Mask10	Mask9	Mask8	
SPIS_CTL	0BH	XX	W	SPIS_CFG [15:0]								SPI Slaver Control
SPIS_DAT	0CH	XX	XX	SPIS_DAT [15:0]								SPI Slaver Data
SPIM_CTL	0DH	XX	R/W	SPIM_CFG [15:0]								SPI Master Control
SPIM_DAT	0EH	XX	R/W	SPIM_DAT [15:0]								SPI Master Data
Reserve	0FH	XX	R/W									
Reserve	10H	XX	R/W									
Reserve	11H	XX	R/W									
Reserve	12H	XX	XX									
Reserve	13H	XX	XX									
Reserve	14H	XX	R/W									
PUPD_PA.L	15H	3F	R/W	-	-	PortA_PULLDOWN[5:0]						PortA PULLDOWN / PULLUP Control
PUPD_PA.H	15H	00		-	-	PortA_PULLUP[5:0]						
Audio-PWML	16H	XX	W	Audio-PWML [15:0]								Audio L Channel
Audio-PWMR	17H	XX	W	Audio-PWMR [15:0]								Audio R Channel
Reserve	18H	XX	R/W									Reserve
Reserve	19H	XX	R/W									Reserve a
PUPD_PB.L	1AH	3F	R/W	-	-	PortB_PULLDOWN[5:0]						PortB PULLDOWN / PULLUP Control
PUPD_PB.H	1AH	00	R/W	-	-	PortB_PULLUP[5:0]						
PUPD_PC.L	1BH	FF	R/W	PortC_PULLDOWN[7:0]								PortC PULLDOWN / PULLUP Control
PUPD_PC.H	1BH	00	R/W	PortC_PULLUP[7:0]								
MISC.L	1CH	00	R/W	0	0	PWM_MUTE	-	RC_RST	EXRST	LVR	WDT	System Reset source come from
MISC.H	1CH	00	R/W	Clr_RealT	-	-	-	-	MODX	LDO33EN	TCS	
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	00	R	RealT[15:0]								Watch Dog Real-Time Counter
IOP_IX	1EH	XX	W	IOPIX[7:0]								Programming IO Port index
IOP_DAT	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.1 Common I/O registers

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.2.3 Basic System Registers

◆STATUS register

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
STATUS.L	00H	20	R/W	INTEN	-	-	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	-	IntPrWR	-	SPIS_EN	SPIM_EN	

The Status register provides two main functions, the first system flag holds the status information generated by the computational blocks of the TxP16E, which used for program sequencer control. The second indicated that special function of hardware module is enable or not.

For program flow control:

System Flag	Definition
AZ	ALU or AR Result Zero
AN	ALU or AR Result Negative
AV	ALU Overflow
AC	ALU Carry
PA	Parser Queue available(Read only)
FA	Filter buffer available(Read only)

System hardware control:

System Flag	Definition
INTEN	System global interrupt control bit
IntVWR	Interrupt Vector Table access window control bit
IntPrWR	Interrupt Priority Table access window control bit
SPIS_EN	SPI slaver interface control bit
SPIM_EN	SPI master interface control bit

◆ Address 01H, 02H and 0AH: Interrupt control registers, the detail are illustrated in Interrupt section.

◆ Address 04H~15H: GPIO registers, the detail are illustrated in GPIO section.

◆Address 16H~17H: Audio-PWM control registers, the detail are illustrated in AUDIO section.

◆System Miscellanea register

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
MISC.L	1CH	00	W/R	0	0	PWM_MUTE	-	RC_RST	EXRST	LVR	WDT	System miscellanea register
MISC.H	1CH	00	R/W	Clr_RealT	-	-	-	-	MODX	LDO33 EN	TCS	

TCS (RealT Timer):

TCS =1: Enable RealT Timer

If programmer read the “RealT” register, it can get 32-bit timer based on **30.517ns(32.768MHz)**. An example is shown as follows.

```
io[RealT]   = ar          ; write to reset the state machine of 32-bit real timer.
ar          = io[RealT]   ; read low-word timer[15:0]
ar          = io[RealT]   ; read high-word timer[31:16]
```

Clr_RealT: Set high to clear 32-bit RealT timer. (this bit only for TCS=1)

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

TCS =0: Disable RealT Timer

LDO33: Enable LDO 3.3V/1.8V power output. *(Note: When user enable LDO power on, user must insert the power on delay program in order to wait the stable LDO power output.)*

MODX: modx=0 is chosen narrowband sound-effect filter.
modx=1 is chosen wideband sound-effect filter.
Actual bandwidth is dependent on source signal sample-rate.

PWM_MUTE: Audio PWM mute enable

RC_RST: System Reset from internal RC reset

EXRST: System Reset from external reset pin

LVR: System Reset from low voltage reset

WDT: System Reset from watch dog reset

Note: RC_RST, EXRST, LVR will clear WDT bits, except for WDT is set to 1. All of the reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device reset.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

◆ Virtual Programming IO

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
VIO_IX	1EH	XX	W	-	-	-	IOPIX4	IOPIX3	IOPIX2	IOPIX1	IOPIX0	Programming IO Port index
VIO_DATA	1FH	XX	W	IOPD[15:0]								Programming IO Port Data

Table 5.2 Virtual Programming IO

The operation steps of these group register, first select virtual IO port index then write data to programming IO port.

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	00	RW	Timer0[15:0]								Timer1
Timer2	01H	00	RW	Timer1[15:0]								Timer2
RTCTimer	02H	00	RW	RTCTimer[15:0]								RTC Timer
PreScale.L	03H	00	W			Timer1_Trig_SEL [1:0]		Timer1_PreScale[3:0]				Timer1 Pre-Scale write
PreScale.H	03H	00	W			Timer2_Trig_SEL [1:0]		Timer2_PreScale[3:0]				Timer2 Pre-Scale write
PreScale.L	03H	00	R	Timer2_PreScale[3:0]				Timer1_PreScale[3:0]				Timer1 Pre-Scale read
PreScale.H	03H	00	R					Timer2_Trig_SEL [1:0]		Timer1_Trig_SEL [1:0]		Timer2 Pre-Scale read
GRTimer	04H	00	RW	GRTimer[12:0]								Green Mode Timer
ODEN_PA	05H	00	RW	PortA_ODEN[5:0]								PortA Open Drain Enable
ODEN_PB	06H	00	RW	PortB_ODEN[5:0]								PortB Open Drain Enable
ODEN_PC	07H	00	RW	PortC_ODEN[7:0]								PortC Open Drain Enable
Reserve	08H	00	RW									
Reserve	09H	00	RW									
CLK_CFG	0AH	00	RW	CLOCK_CONFIG[13:0] (see 7.3.3.2)								CLOCK Configuration
CLK_DAT1	0BH	00	RW	CLOCK_DATA1[15:0] (see 7.3.3.2)								CLOCK Data Access1
CLK_DAT2	0CH	00	R	CLOCK_DATA2[15:0] (see 7.3.3.2)								CLOCK Data Access2
PDSEL_PA	0DH	00	W	PortA_PDSEL[5:0]								PortA I/O PullDown R Select “1”= 500K, “0” = 100K of related PA bit
PDSEL_PB	0EH	00	W	PortB_PDSEL[5:0]								PortB I/O PullDown R Select “1”= 500K, “0” = 100K of related PB bit
PDSEL_PC	0FH	00	W	PortC_PDSEL[7:0]								PortC I/O PullDown R Select “1”= 500K, “0” = 100K of related PC bit
WAKEN_PA	10H	00	W	PortA_WAKEN[5:0]								PortA WAKE UP Enable
WAKEN_PB	11H	00	W	PortB_WAKEN[5:0]								PortB WAKE UP Enable
WAKEN_PC	12H	00	W	PortC_WAKEN[7:0]								PortC WAKE UP Enable
WAKELV_PA	13H	00	W	PortA_WAKELV[5:0]								PortA WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PA bit
WAKELV_PB	14H	00	W	PortB_WAKELV[5:0]								PortB WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PB bit
WAKELV_PC	15H	00	W	PortC_WAKELV[7:0]								PortC WAKE UP Edge “1”= Pos-Edge, “0” = Neg-Edge of related PC bit
WAKEDLV_PB	16H	00	W	PortB_WAKEDLV[3:0]								PortB Double-Edge WAKE UP Enable
CUR_PWM	17H	0C	RW	CUR_PWM[3:0]								PWM I/O PAD Driving Current
Reserve	18H											
Reserve	19H											

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.3 PC Stack

The PC STACK is TxP16E special embedded memory used to save (PC+1) value, which is composed with 24-level.

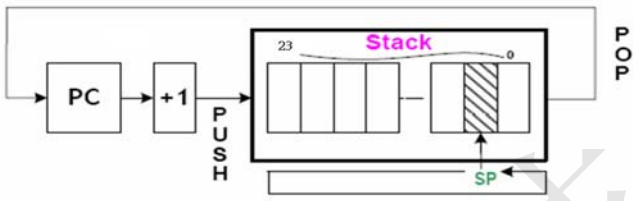


Figure 5.3 PC Stack Structure

Stack's top value is indexed by stack pointer (SP) register. When CALL instruction is executed, then the (PC+1) will PUSH onto stack addressing by SP and it will auto decrement. At the end of subroutine when RETS instruction is executed the SP will auto increment and stack content of pointer by SP will POP into PC.

The contents of STACK and SP are neither readable nor writeable by instruction. The SP is initialized to “0” after RESET.

5.4 Interrupt

5.4.1 Interrupt Vector Table

The Interrupt Vector Table is TxP16E special embedded memory, which is composed with 16-level of FIFO, used to store the index of interrupt service routine (ISR) address. User can access Interrupt Vector Table by read/write IntVect I/O register, which refers PCB register to compose of 18-bit address.

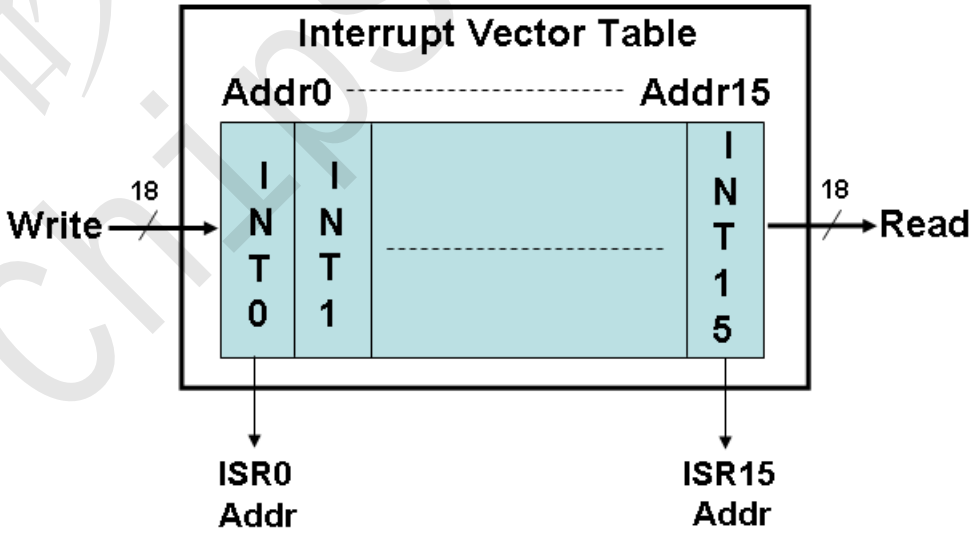


Figure 5.4 Interrupt Vector Structure

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.4.2 Interrupt Controller

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS	00H	00	R/W	INTEN				AN	AV	AC	AZ	System Status Flag
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Int Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Int Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	
INTMASK.L	0AH	00	R/W	Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0	Interrupt Mask
INTMASK.H	0AH	00	R/W	0	Mask14	Mask13	Mask12	Mask11	Mask10	Mask9	Mask8	

This chip provides several interrupt sources, including internal Audio PWM, T1, T2, RTC, SPI master, PC Stack Overflow, SPI slaver, Flash ready, ADC, TRA1402, and 2 external ExtINT0, ExtINT1, interrupts, and NMI interrupt. More details control will describe as follows:

Interrupt Source	Interrupt Vector	Priority(default)
Audio PWM Timer	0H	INT0_IRQ
Timer1	1H	INT1_IRQ
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0	4H	INT4_IRQ
ExtINT1	5H	INT5_IRQ
SPI Master	6H	INT6_IRQ
PC Stack Overflow	7H	INT7_IRQ
SPI Slaver	8H	INT8_IRQ
Flash Erase/Program Ready	9H	INT9_IRQ
ADC	AH	INT10_IRQ
Reserve	BH	INT11_IRQ
Reserve	CH	INT12_IRQ
TRA1402	DH	INT13_IRQ
Reserve	EH	INT14_IRQ(lowest)
NMI(Non-Mask Interrupt)	FH	INT15_IRQ(highest)

Table 5.3 Interrupt Sources

(a) Global interrupt enable(INTEN)

The global interrupt INTEN controls the enable/disable of all interrupts. When INTEN is cleared to “0”, all interrupts are disabled. When INTEN is set to “1”, all interrupts are enabled (but still dependent on value of INTENA register). The INTEN is initialized to “”0” after power on.

(b) Interrupt enable (INTENA)

The interrupt enable from ENA15 to ENA0 are shown in above. An interrupt is allowed when these control bit are set to “1”, and interrupt is inhibit when these control bit are cleared to “0”. They are all initialized to “0” after power on.

(c) Interrupt request (INTREQ)

If an interrupt raising edge request is generated, the related interrupt request bit is set to “1” by hardware and waits for interrupt accept. INTREQ can be cleared to “0” by software. Hardware will not clear this bit. INTREQ are all initialized to “0” after power on.

(d) Interrupt mask (INTMASK)

The interrupt can be masked by setting Mask[14:0] interrupt mask register as above. Each interrupt source in the system can be masked individually except NMI.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

(e) Programmable Interrupt Priority

INT15_IRQ (highest) > INT0_IRQ > INT1_IRQ > INT2_IRQ > INT3_IRQ > INT4_IRQ > INT5_IRQ > INT6_IRQ > INT7_IRQ > INT8_IRQ > INT9_IRQ > INT10_IRQ > INT11_IRQ > INT12_IRQ > INT13_IRQ > INT14_IRQ(lowest). Interrupt Priority can be programmable, user can re-arrange any interrupt source to wanted interrupt priority except NMI. For Example, user can assign SPI Slaver interrupt source to INT14_IRQ, and then SPI Slaver interrupt priority will be changed to lowest level.

For Example: Exchange ADC priority with Timer1 priority

Assign ADC interrupt source to INT1_IRQ(Interrupt Vector: 1H) and assign Timer1 interrupt source to INT10_IRQ(Interrupt Vector: AH), than ADC priority will be higher than Timer1 priority.

Interrupt Source	Interrupt Vector	Priority(default)
Audio PWM Timer	0H	INT0_IRQ
ADC	***1H***	***INT1_IRQ***
Timer2	2H	INT2_IRQ
RTC Timer	3H	INT3_IRQ
ExtINT0	4H	INT4_IRQ
ExtINT1	5H	INT5_IRQ
SPI Master	6H	INT6_IRQ
PC Stack Overflow	7H	INT7_IRQ
SPI Slaver	8H	INT8_IRQ
Flash Erase/Program Ready	9H	INT9_IRQ
Timer1	***AH***	***INT10_IRQ***
Reserve	BH	INT11_IRQ
Reserve	CH	INT12_IRQ
TRA1402	DH	INT13_IRQ
Reserve	EH	INT14_IRQ(lowest)
NMI(Non-Mask Interrupt)	FH	INT15_IRQ(highest)

(f) Configurable NMI Interrupt Source

NMI interrupt source can be programmable. User can assign any interrupt source as NMI interrupt source. For Example, user can assign SPI Slaver interrupt source to NMI(INT15_IRQ), and then SPI Slaver interrupt priority will be changed to highest level.

5.4.3 Interrupt Processing

When any interrupt request(INTREQ) is generated, the acceptance of interrupt is decided by the interrupt enable(ENA) and global interrupt enable(INTEN). If the global interrupt enable(INTEN), related interrupt enable bit(ENA) are set to “1” and related mask bit(MASK) are cleared to 0, that interrupt will be accepted on the next clock. These following procedures will automatically be done in one clock cycle by hardware showing below:

(1) Program Counter(PC), PCB, PCH, AR and FLAG will be stored in special hardware registers.

(2) PC will be set to the corresponding interrupt entry address by refer to interrupt vector table.

(3) The global interrupt enable (INTEN) is cleared to “0”, which avoids the nest interrupt happened.

When interrupt service routine was finished, an RETI instruction will perform the procedures by hardware

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

showing as follows:

(1) Restore the stored PC, PCB, PCH, AR and FLAG.

(2) The global interrupt enable (INTEN) is set to “1”, which allows to accept the subsequent interrupt.

Before executing RETI instruction, the corresponding interrupt request (INTREQ) bit must be cleared to “0” by software. If the request bit is not cleared, the same interrupt will be accepted again.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.5 MAC (16-bit X 16-bit Multiplier and Accumulator)

A 16 bit x 16 bit MAC is provided for digital signal processing. The core of MAC operation is multiply MX&MY with 2'S complement operand and accumulation previous 40-bit MF then rounding store result in the 40-bit MR register. The basic MAC architecture is shown as Figure 5.5.

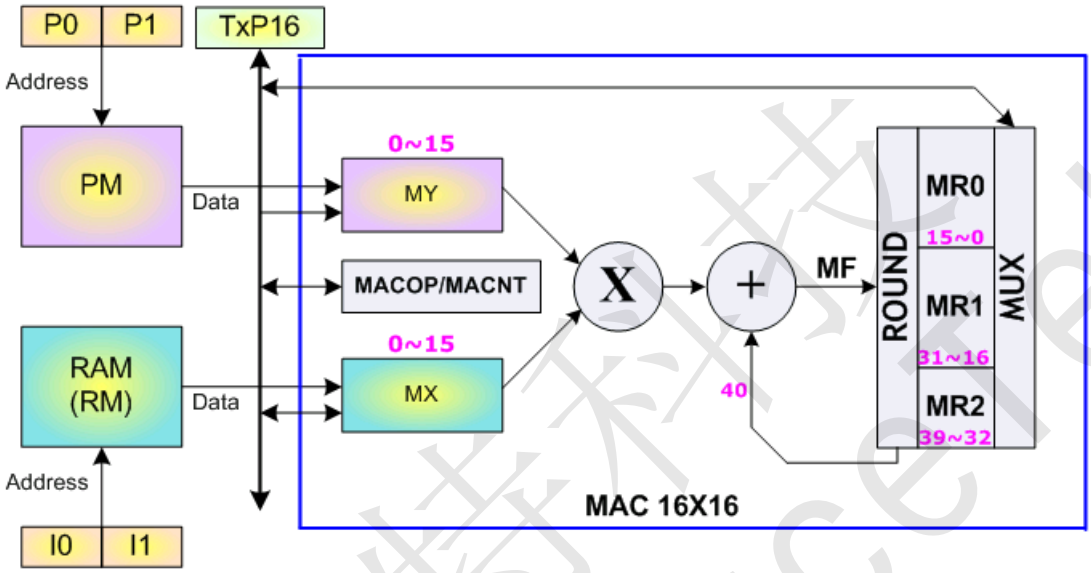


Figure 5.5 MAC Architecture

Define MAC module registers:

MX: MAC input 16-bit X register

MR: Multiplier or MAC result 40-bit register

MACOP: MAC operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup

MACNT: MAC equation loop counter, max to 255

Basically, multiplier operates equation:

MR = MX*MY(SU) → MX: signed, MY: unsigned

Permission MY is AR or immediate value (-128~127), MX and MY are signed or unsigned assign by MACOP. So, actual multiplier instruction likes this:

MR = MX*AR or MR = MX*56

The operation of MAC equation is:

MR = MR + (MX*MY(SU))<<RND, MX=RM[I0++], MY=PM[P1--]

The means of equation is signed MX multiply unsigned MY the result value shift left RND bits and add previous MR then write back to MR.

Simultaneously, load new value to MX fixed from RM[index operation]

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

MY fixed from PM[pointer operation]

Therefore, MAC array operation like this:

```
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
                .
                .                                          Successive 64 times
                .
MR = MR + ( MX*MY(SS) ) << 1, MX=RM[I0++], MY=PM[P1--]
```

Actual just one line of instruction present in assembly coding like this:

MACNT = 63

This is very benefit for reducing code size. Of curse, we need setup MACOP register previous; at this example is like this;

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
MACOP	00	R/W	RND1	RND0	P0/P1	POP:+/-	I0/I1	IOP:+/-	MY:SU(01)	MX:SU(01)	MAC Operation Setup
			0	1	1	1	0	0	0	0	

Note: Successive MAC operation will cause MCU interrupt disable.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

5.6 Barrel Shifter

The shifter accept a 16-bit input and can any place in a 32-bit output. The core of shifter include arithmetic shift, logic shift, exponent detector and normalization. The basic shifter architecture is shown as Figure 5.6.

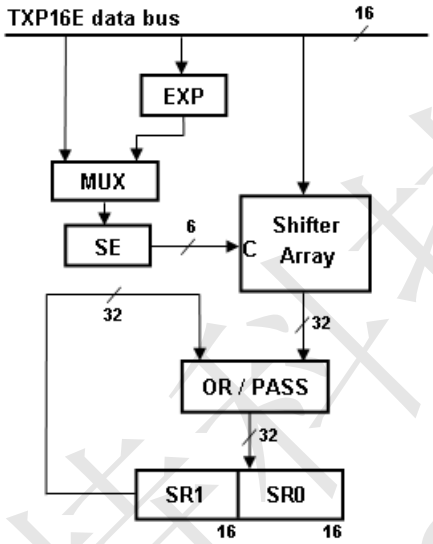


Figure 5.6 Barrel Shifter Architecture

Define Barrel Shifter module registers:

EXP: The EXP (Exponent Detector) register determines the number of leading sign bits and produces output number which indicates to eliminate redundant sign bits during the normalize operation.

SE: The shifting of input is determined by SE register. Positive SE value indicates a left shift and negative SE value indicate a right shift. SE register is set from TxP16E bus or EXP register.

SR1, SR0: barrel shifter result 32-bit register

SFTOP: shifter operation define register

Symbol	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
SFTOP	00	W							Arith./Logic	PASS/OR	Shifter Operation Setup

SFTOP[1]: 0(arithmetic shifter, default), 1(logic shifter).

SFTOP[0]: 0(the shifter array output is passed through and load to SR register), 1(shifter array output may be OR logic with SR register, and then OR logic result is loaded into SR register).

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

6. TR16F032A/B Memory Configuration

6.1 Internal Program/Parameter Memory

TxP16E consider both instruction and data ROM are the same as program ROM(PM), so it's very flexible and efficient for instruction and data memory allocation in PM. The total of logical PM space is 4 banks. Each bank has 64 K space. The 4 x 64K space is addressed by memory address generator unit (MAG). The BANK0 and BANK2 are implemented as Flash memory and static RAM, respectively. The DFF register starts at the last location of BANK0 (0FFF0h~0FFFFH), and user can dynamically update PM data for MAC operation. More details control will describe as follows:

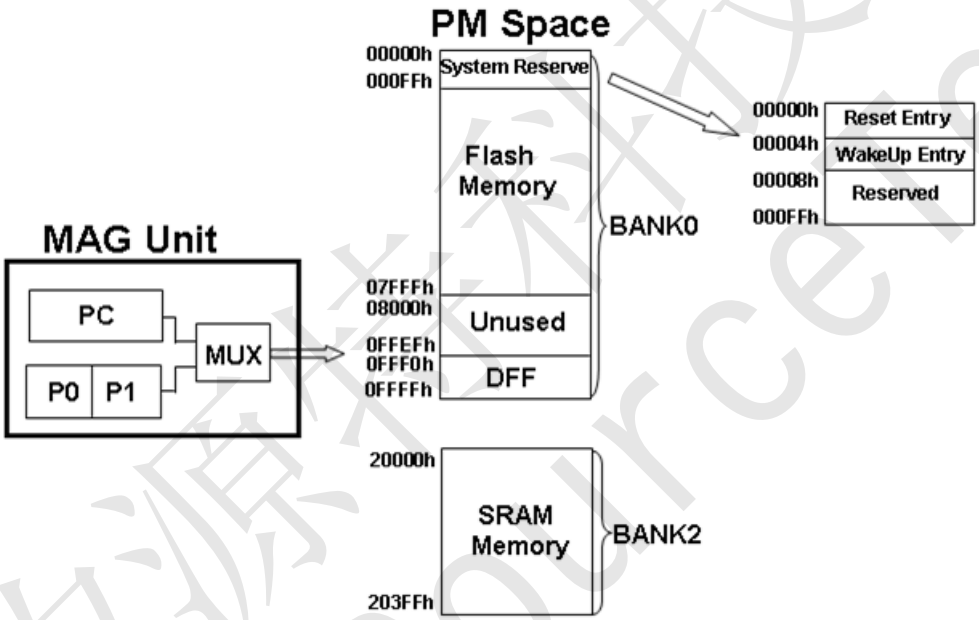


Figure 6.1 PM block diagram

When TxP16E executed an instruction, the PM address is generated from PC register. Similarity, when it access a word data, the PM address is composed with 18-bit from P0 or P1. System will auto adjust execute target space when program context switch between BANK0 and BANK2.

6.2 Internal Data Working SRAM

The internal data working ram space is totally 4Kx16-bit that named as RM. Addressing ranged from 0x0000 through 0x0FFF, which is generated by Data Address Generator Unit (DAG). Note: Index register (I0,I1,BP) are 16-bit width, but RM address line is only 12-bit width(0~4095); therefore, RM address will be warping when index value exceed 4095.

Note: Total SARM size is 4Kx16-bit. If PM(BANK2 / 1Kx16-bit) is used, RM will be 3Kx16-bit. If PM(BANK2) is no used, RM will be 4Kx16-bit. SARM configuration is set by option code.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

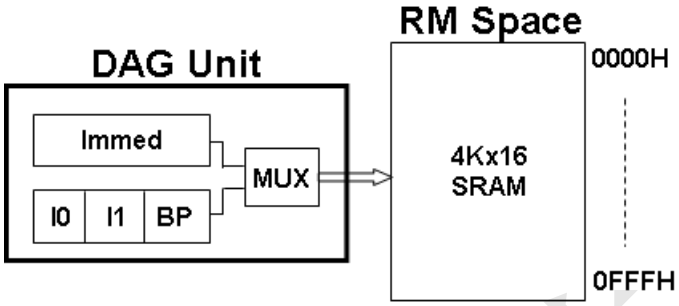


Figure 6.2 RM block diagram

6.3 Data Stack

A Last In First Out (LIFO) STACK is implementation for temporary data storage in RM memory. Generally, Data Stack is start-up at the bottom of RM, so BP is usually set to 0x0FFF.

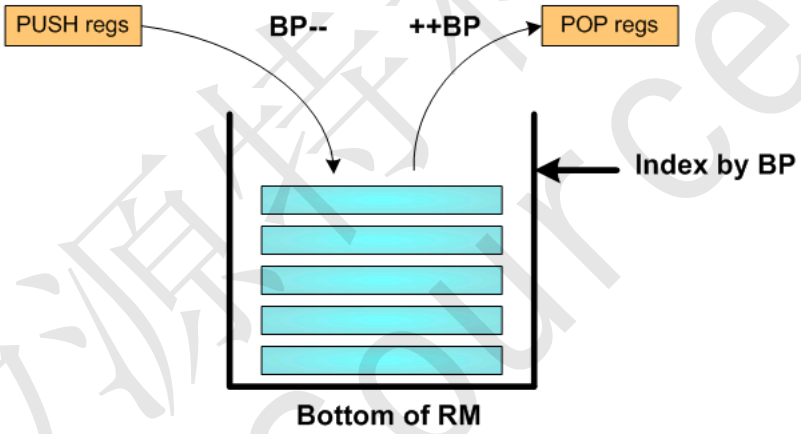


Figure 6.3 Data Stack Structure

Data Stack's top value is indexed by base pointer (BP) register. When PUSH instruction is executed, the “regs” will PUSH onto stack which address by BP and it will auto decrement. If POP instruction is performed, the BP will auto increment and stack content of pointed by BP will POP into “regs”.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7. TR16F032A/B Peripherals

7.1 Programmable Timers

Common I/O registers

Symbol	Adr	Reset	RW	B7	B6	B5	B4	B3	B2	B1	B0	Description
STATUS.L	00H	20	R/W	INTEN	OSC_EN	-	AQ	AN	AV	AC	AZ	System Status Flag
STATUS.H	00H	00	R/W	PA	FA	IntVWR	0	IntPrWR	0	SPIS_EN	SPIM_EN	
INTENA.L	01H	00	R/W	ENA7	ENA6	ENA5	ENA4	ENA3	ENA2	ENA1	ENA0	Interrupt Enable
INTENA.H	01H	00	R/W	ENA15	ENA14	ENA13	ENA12	ENA11	ENA10	ENA9	ENA8	
INTREQ.L	02H	00	R/W	Req7	Req6	Req5	Req4	Req3	Req2	Req1	Req0	Interrupt Request
INTREQ.H	02H	00	R/W	Req15	Req14	Req13	Req12	Req11	Req10	Req9	Req8	

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
Timer1	00H	00	RW	Timer0[15:0]								Timer1
Timer2	01H	00	RW	Timer1[15:0]								Timer2
RTCTimer	02H	00	RW	RTCTimer[15:0]								RTC Timer
PreScale.L	03H	00	W			Timer1_Trig_SEL [1:0]	Timer1_PreScale[3:0]					Timer1 Pre-Scale write
PreScale.H	03H	00	W			Timer2_Trig_SEL [1:0]	Timer2_PreScale[3:0]					Timer2 Pre-Scale write
PreScale.L	03H	00	R	Timer2_PreScale[3:0]			Timer1_PreScale[3:0]					Timer1 Pre-Scale read
PreScale.H	03H	00	R					Timer2_Trig_SEL [1:0]		Timer1_Trig_SEL [1:0]		Timer2 Pre-Scale read
GRTimer	04H	00	RW	GRTimer[12:0]								Green Mode Timer

7.1.1 Audio PWM Timer

Audio PWM timer is fixed generate 32kHz interrupt request when INTENA0 bit is turned on, *If Auto FIFO_EN is setting the interrupt request rate = Ft / FIFO_Length.* ***Notice: It should be avoided that INTENA bit0 is turned on/off quickly. If need to turned on/off INTENA bit0 quickly, recommend to use INTMASK bit0. About detail, please refer to "FDSP programming guide".***

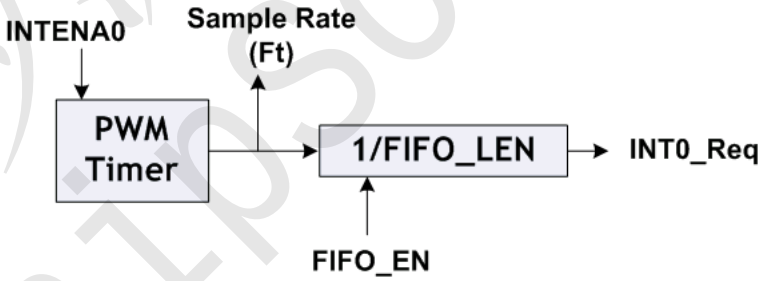


Figure 7.1 Audio PWM Timer Structure

7.1.2 Timer1 & Timer2

The clock source of Timer1 & Timer2 comes from fixed 32.768Mhz or External Clock Input, It contains 16-bit write-only counter register. If Timer enable correspond with the INTENA bit is turned on then counting to time out, an interrupt request will be generated. At the same time, TnC in Eq.(7.1.1) will be reloaded into Timer register and up-count again. If the global interrupt enable, an interrupt signal is generated at the next clock.

The N is prescale parameter, N range can be 1, 2, 4, 8, 16, 32, 64, 128, 256. Clock Source of timer is the frequency of 32.768MHz or External clock input divided by N.

Int1_Req / Int2_Req = (32.768Mhz / N) / (TnC+1) or

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Int1_Req / Int2_Req = (External Clock Input / N) / (TnC+1)

Timer1_prescale[3:0]	Timer2_prescale[3:0]	N
0	0	1
1	1	1
2	2	1
3	3	1
4	4	1
5	5	1
6	6	1
7	7	1
8	8	2
9	9	4
10	10	8
11	11	16
12	12	32
13	13	64
14	14	128
15	15	256

Timer Pre-scale Table

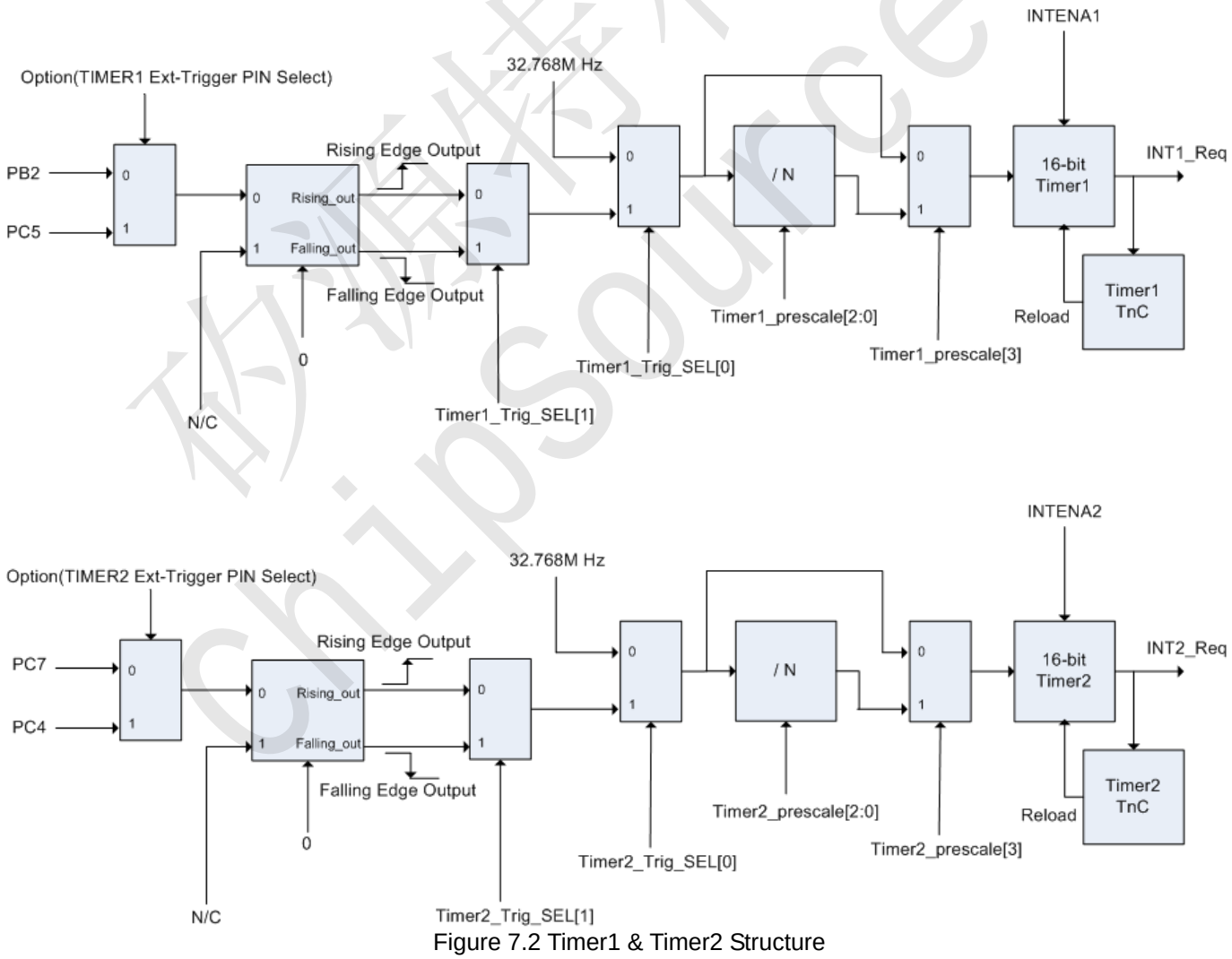


Figure 7.2 Timer1 & Timer2 Structure

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.1.3 RTC(Real Time Clock) Timer

The RTC Timer input frequency can select 32K XTAL(32768Hz) or Low power RC oscillator 32768Hz ± 2% (LP32K) by option. It contains 16-bit counter register. RTC generates interrupt request or wake-up MCU when in halt mode or interrupt in normal mode. The wake-up function can be disabled by option.

The frequency of Int3_Req = 32768Hz / (RTC Timer TnC+1)

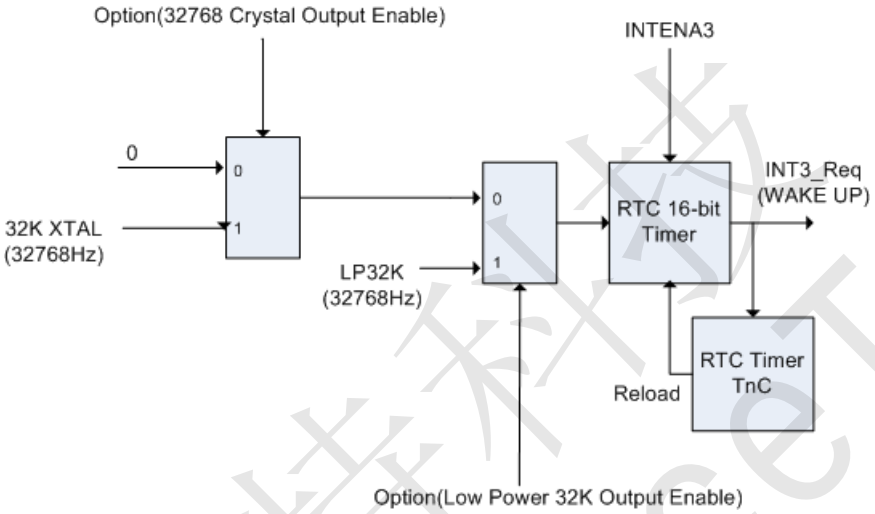


Figure 7.3 RTC Timer Structure

7.1.4 Green Mode Timer (GRTimer)

The Green Mode Timer input frequency can select 32K XTAL(32768Hz) or Low power RC oscillator 32768Hz ± 2% (LP32K) by option. It contains 13-bit counter register. GRTimer generates wake-up MCU signal when in green mode. GRTimer range is from 0 to 0x1ffe. If GRTimer value is larger, working frequency at green mode is slower.

The frequency of green mode ≒ 32768Hz / (GR Timer TnC+4.06448)

Note: If green mode function is executed, RTC wakeup in halt mode/Green mode of IDE option need to be enabled.

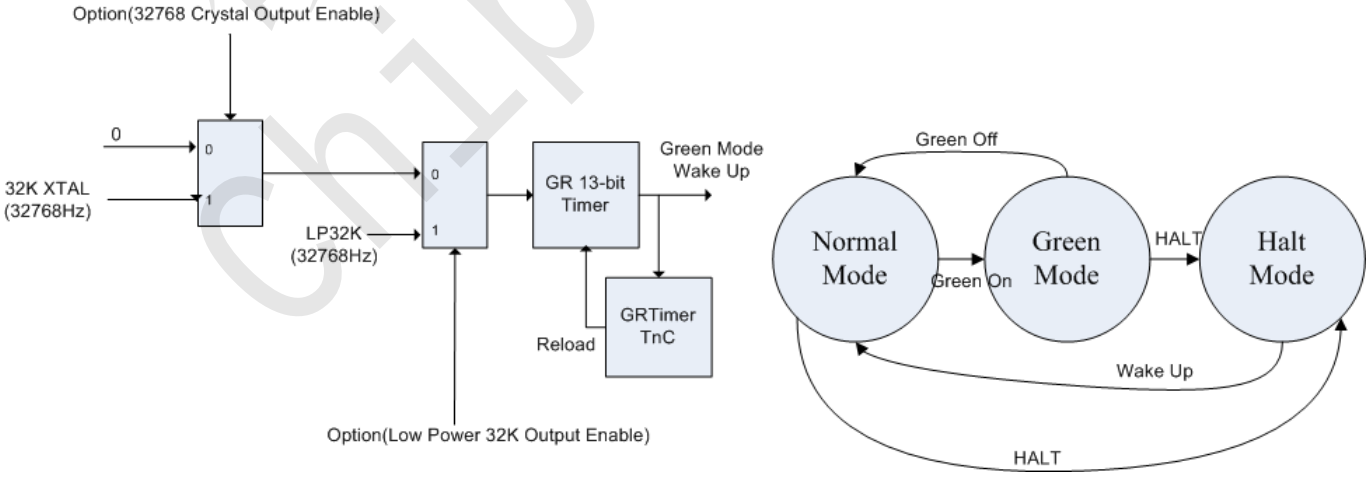


Figure 7.4 Green Mode Timer Structure & state diagram between the different modes

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.2 General Purpose I/O Ports

The TR16F032 provides 4 I/O ports for user application. There are four I/O port, PA0~PA5, PB0~PB5, PC0~PC7 and PI0~PI1. The input/output bits programmable by IOC control register respectively. PA0~PA5, PB0~PB5, PC0~PC7 wake-up function enable or disable by user program, and (PB3/PC6,PC3/PB1) are external interrupt pin. The pull-up 100K or pull-down 100K/500K resistor of each pin can be programmed by user program(Common I/O register : PUPD_PA, PUPD_PB, PUPD_PC). The pull-down 100K or pull-down 500K resistor of each pin can be programmed by user program(Virtual Programming IO Port : PDSEL_PA, PDSEL_PB, PDSEL_PC). Each pin can be configured to open-drain pad by user program. The basic I/O schematic is showed in Figure 7.5.

Common I/O registers

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
IOC_PA	04H	00	R/W	IOC_PA[5:0]								"1"= out, "0" = in of related PA bit
IOC_PB	05H	00	R/W	IOC_PB[5:0]								"1"= out, "0" = in of related PB bit
IOC_PCI.L	06H	00	R/W	IOC_PC[7:0]								"1"= out, "0" = in of related PC bit
IOC_PCI.H	06H	00	R/W	IOC_PI[1:0]								1"= out, "0" = in of related PI bit
PortA	07H	XX	R/W	PortA[5:0]								Read: in port Write: out port
PortB	08H	XX	R/W	PortB[5:0]								Read: in port Write: out port
PortCI.L	09H	XX	R/W	PortC[7:0]								Read: in port Write: out port
PortCI.H	09H	XX	R/W	PortI[1:0]								Read: in port Write: out port
PUPD_PA	15H	XX	XX	PortA_PULLUP[5:0]				PortA_PULLDOWN[5:0]				
PUPD_PB	1AH	XX	XX	PortB_PULLUP[5:0]				PortB_PULLDOWN[5:0]				
PUPD_PC	1BH	XX	XX	PortC_PULLUP[7:0]				PortC_PULLDOWN[7:0]				

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
ODEN_PA	05H	00	RW	PortA_ODEN[5:0]								PortA Open Drain Enable
ODEN_PB	06H	00	RW	PortB_ODEN[5:0]								PortB Open Drain Enable
ODEN_PC	07H	00	RW	PortC_ODEN[7:0]								PortC Open Drain Enable
PDSEL_PA	0DH	00	W	PortA_PDSEL[5:0]								PortA I/O PullDown R Select "1"= 500K, "0" = 100K of related PA bit
PDSEL_PB	0EH	00	W	PortB_PDSEL[5:0]								PortB I/O PullDown R Select "1"= 500K, "0" = 100K of related PB bit
PDSEL_PC	0FH	00	W	PortC_PDSEL[7:0]								PortC I/O PullDown R Select "1"= 500K, "0" = 100K of related PC bit
WAKEN_PA	10H	00	W	PortA_WAKEN[5:0]								PortA WAKE UP Enable
WAKEN_PB	11H	00	W	PortB_WAKEN[5:0]								PortB WAKE UP Enable
WAKEN_PC	12H	00	W	PortC_WAKEN[7:0]								PortC WAKE UP Enable
WAKELV_PA	13H	00	W	PortA_WAKELV[5:0]								PortA WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PA bit
WAKELV_PB	14H	00	W	PortB_WAKELV[5:0]								PortB WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PB bit
WAKELV_PC	15H	00	W	PortC_WAKELV[7:0]								PortC WAKE UP Edge "1"= Pos-Edge, "0" = Neg-Edge of related PC bit

These totally 22 I/O pins work not only just a general input/output port function but also can be configured as SPI master/slaver, ADC analog input, TRA1402 interface, Microphone, External Crystal. For more detail please refer to relative section.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

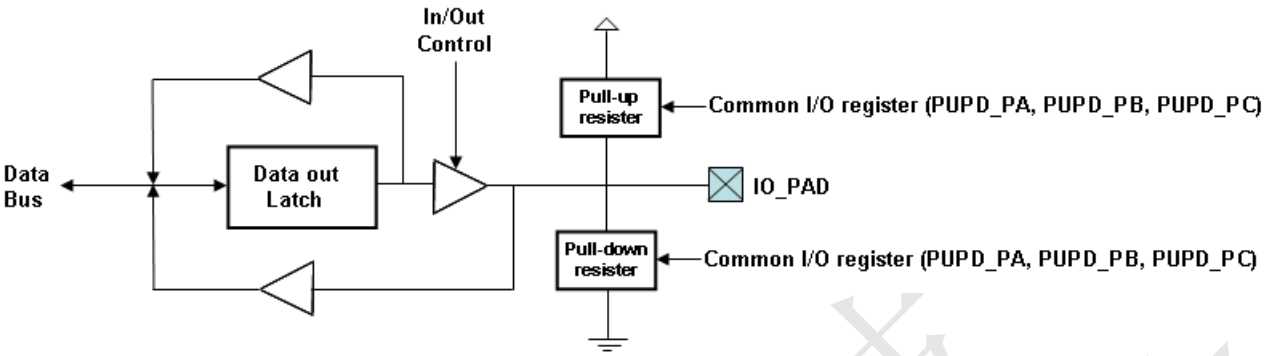


Figure 7.5 Basic I/O Configuration

PB0, PB1, PB2 and PB3 support two edge modes for wake-up function are rising and falling edge trigger. The rising and falling edge trigger is selected by user program.

Virtual Programming IO Port

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	B12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
WAKEDLV_PB	16H	00	W	PortB_WAKEDLV[3:0]								PortB Double-Edge WAKE UP Enable

The PortB0, PortB1, PortC6, PortC7 also provides 2 comparators configuration for user application that each comparator enable or disable by option.

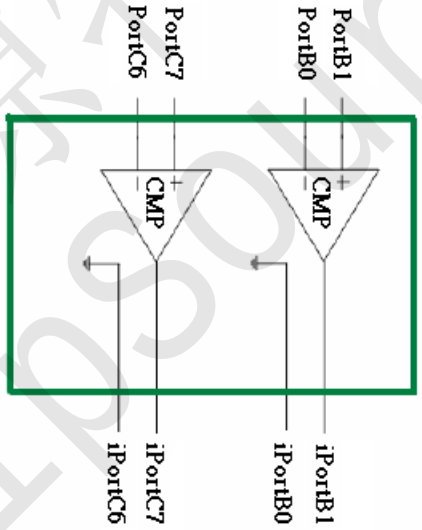


Figure 7.6 Comparator Configuration

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3 Extension Device

TR16F032 built-in special hardwires for external device connection capability are listed below:

7.3.1 SPI Master Controller

In order to enable SPI Master Controller interface, user should set STATUS.b8 = 1 before SPI Master Controller operation.

7.3.1.1 Features

- Support DMA read/write data
- Support 4-bit Serial Flash
- Serial clock rate: 32.768 MHz / 16.384 MHz / 13.107 MHz / 10.922 MHz / 8.192 MHz / 4.096 MHz
- Built in 4x16 bits data buffer

I/O Port	SPI interface	Direction	Description
PortA.5	SIO3	I/O	Serial Data3 input/output (Quad mode)
PortA.4	SIO2	I/O	Serial Data2 input/output (Quad mode)
PortA.3	SO/SIO1	I/O	Serial Data output (1xI/O mode) or Serial Data1 input/output (Quad mode or Dual mode)
PortA.2	SI/SIO0	I/O	Serial Data input (1xI/O mode) or Serial Data0 input/output (Quad mode or Dual mode)
PortA.1	SCK	O	Serial Clock
PortA.0	CS	O	Chip Select(free assign by user)

7.3.1.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	0DH	01	W	-	CLR	RCV	SEND	Total Send/Receive Byte				Control Register Low Byte
CTRL_W.H	0DH	00	W	Mode	CKSEL			ICS	-	Dual_ Quad_SEL	Dual_ Quad_EN	Control Register High Byte
CTRL_R.L	0DH	00	R	DATOK	CLR	RCV	SEND	Total Send/Receive Byte				Read Status Low Byte
CTRL_R.H	0DH	00	R	Mode	CKSEL			ICS	-	Dual_ Quad_SEL	Dual_ Quad_EN	Read Status High Byte

Total Send/Receive Byte: Total byte number of sending or receiving.

ICS: Internal SPI command select enable.

SEND: Trigger sending data.

RCV: Trigger receiving data.

CLR: Clear control flag.

CKSEL: (000: 32.768MHz), (001: 16.384MHz), (010: 13.107 MHz), (011: 10.922 MHz), (100: 8.192 MHz), (101: 4.096 MHz).

Mode: (0:Posedge latch data), (1:Negedge latch data).

DATOK: Indicate transmit/receive data O.K.

DUAL_QUAD_EN: 1 -> Dual_Quad Enable 0 -> Dual_Quad Disable

DUAL_QUAD_SEL: 1 -> Quad Mode 0 -> Dual Mode

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W	0EH	XX	W	DATA[15:0]								Write Transmission Data Value
DATA_R	0EH	XX	R	DATA[15:0]								Read Received Data Value

DATA [15:0]: Transmit/Receive Data Value

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.1.3 DMA Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	53H	00	W	-	-	-	SET_CONTROL_MODE	DMA_AUTO_RSET	DMA_DIR	DMA_EN	-	Control Register Low Byte
CTRL_W.H	53H	00	W	-	-	-	-	-	-	-	-	Control Register High Byte
CTRL_R.L	53H	00	R	-	-	-	-	-	DMA_DIR	DMA_EN	DMA_BUSY	Read Status Low Byte
CTRL_R.H	53H	00	R	-	-	-	-	-	-	-	-	Read Status High Byte

DMA_BUSY: Indicate DMA transmitting/receiving data now.

DMA_EN: 1-> DMA Enable, 0->DMA Disable

DMA_DIR: 1-> DMA Direction, From SPI to RM SRAM, 0-> From RM SRAM to SPI

DMA_AUTO_RESET: 1-> the index address of DMA SRAM will be auto reset when DMA transmitting/receiving data completed.

SET_CONTROL_MODE: 1-> Enable setting control mode.

1. If SET_CONTROL_MODE is set to high, user can change another mode by setting bit15 of CTRL_W register. If set bit15 of CTRL_W register to high, improved control mode is choose.
2. If set bit15 of CTRL_W register to low, old control mode is choose.

Improved control mode is that user can access SPI data, don't need to polling DATOK.

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
SPI_ RADR.L	54H	XX	W	SPI_RADR[7:0]								RM SRAM starting address for DMA
SPI_ RADR.H	54H	XX	W	-	-	SPI_RADR[13:8]						
SPI_ DMANUM.L	55H	00	W/R	SPI_DMANUM[7:0]								Set the length of DMA transfer
SPI_ DMANUM.H	55H	00	W/R	-	-	-	-	SPI_DMANUM[11:8]				

After SPI_DMANUM register is written, DMA transfer is issued. The number of SPI_DAMNUM is up to 0x0fff (4K words length).

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.2 SPI Slaver Controller

In order to enable SPI Slave Controller interface, user should set STATUS.b9 = 1 before SPI Slave Controller operation.

7.3.2.1 Features

- Support Input Serial clock rate (Max): 32.768 MHz
- Built in ping-pong data buffer to improve transfer efficiency

I/O Port	SPI interface	Direction	Description
PortC.7	SO	O	Serial Data output
PortC.6	SI	I	Serial Data input
PortC.5	SCK	I	Serial Clock input
PortC.4	CS	I	Chip Select

7.3.2.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.L	0BH	00	W	-	-	-	-	-	Overrun Error Check Enable	MODE_SEL[1:0]		Write Control Register Low Byte
CTRL_R.L	0BH	00	R	-	-	-	CS	Overrun Error -	Overrun Error Check Enable	MODE_SEL[1:0]		Read Control Register Low Byte

MODE_SEL[1:0]: Word/Byte Mode Select (10: Word Mode Enable , 01:Byte Mode Enable)

Overrun Error Check Enable: Enable Check RX buffer Overrun Error.

Overrun Error: RX buffer Overrun Error happen.

CS: user program can read CS(PortC.4) status through this bit.

TX, RX Byte/Word Mode Mapping Table:

MODE_SEL[1:0]	TX	RX
00	N/A	N/A
01	Byte Mode	Byte Mode
10	Word Mode	Word Mode
11	N/A	N/A

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
DATA_W	0CH	XX	W	DATA[15:0]								Write Transmission Data Value
DATA_R	0CH	XX	R	DATA[15:0]								Read Received Data Value

DATA [15:0]: Transmit/Receive Data Value

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.3 CPU Array

CPU Array can combine with several DSP chips by SPI interface, in order to enhance computing power on the application system.

7.3.3.1 Features

- Three channels are available totally.
- Every channel can be set to SPI master or SPI slaver individually.
- Support wire function with any two channels

I/O Port	SPI interface	Direction	Description
PortA.3	SO	I (SPI Master) / O(SPI Slaver)	Serial Data output of Channel A
PortA.2	SI	O(SPI Master) / I(SPI Slaver)	Serial Data input of Channel A
PortA.1	SCK	O(SPI Master) / I(SPI Slaver)	Serial Clock input of Channel A
PortA.0	CS	O(SPI Master) / I(SPI Slaver)	Chip Select of Channel A
PortB.3	SO	I (SPI Master) / O(SPI Slaver)	Serial Data output of Channel B
PortB.2	SI	O(SPI Master) / I(SPI Slaver)	Serial Data input of Channel B
PortB.1	SCK	O(SPI Master) / I(SPI Slaver)	Serial Clock input of Channel B
PortB.0	CS	O(SPI Master) / I(SPI Slaver)	Chip Select of Channel B
PortC.7	SO	I (SPI Master) / O(SPI Slaver)	Serial Data output of Channel C
PortC.6	SI	O(SPI Master) / I(SPI Slaver)	Serial Data input of Channel C
PortC.5	SCK	O(SPI Master) / I(SPI Slaver)	Serial Clock input of Channel C
PortC.4	CS	O(SPI Master) / I(SPI Slaver)	Chip Select of Channel C

7.3.3.2 Control Registers

Symbol	Adr	Reset	RW	b15/b7	B14/b6	b13/b5	b12/b4	b11/b3	B10/b2	b9/b1	b8/b0	Description
CTRL_W.H	0BH	00	W	cpu_ array_ en	array_ wire_ config[2]	array_ wire_ config[1]	array_ wire_ config[0]	array_ slaver_ config[1]	array_ slaver_ config[0]	array_ master_ config[1]	array_ master_ config[0]	Write Control Register High Byte
CTRL_R.H	0BH	00	R	cpu_ array_ en	array_ wire_ config[2]	array_ wire_ config[1]	array_ wire_ config[0]	array_ slaver_ config[1]	array_ slaver_ config[0]	array_ master_ config[1]	array_ master_ config[0]	Read Control Register High Byte

cpu_array_en :

0(cpu array disable) 1(cpu array enable)

array_wire_config[2:0]:

000: disable, 001:connect PortA[3:0] to PortB[3:0] , 010:connect PortB[3:0] to PortA[3:0]
011:connect PortB[3:0] to PortC[7:4] , 100:connect PortC[7:4] to PortB[3:0]
101:connect PortC[7:4] to PortA[3:0] , 110:connect PortA[3:0] to PortC[7:4]

array_slaver_config[1:0]:

00: disable, 01: PortA[3:0] is set to SPI Slaver, 10:PortB[3:0] is set to SPI Slaver,
11:PortC[7:4] is set to SPI Slaver.

array_master_config[1:0]:

00: disable, 01: PortA[3:0] is set to SPI Master, 10:PortB[3:0] is set to SPI Master,
11:PortC[7:4] is set to SPI Master.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Example:

PortA[3:0] of CHIP1 is configured to SPI master, and through PortB[3:0] of CHIP2 to PortC[7:4] of CHIP2, and PortC[7:4] of CHIP2 is connected to PortA[3:0] of CHIP3 (SPI slaver) in this example. CHIP1 can communicate with CHIP3 and go through CHIP2. CHIP2 can monitor the communication data of CHIP1 between CHIP2.

Figure 7.7 is the CPU array connecting diagram of this example.

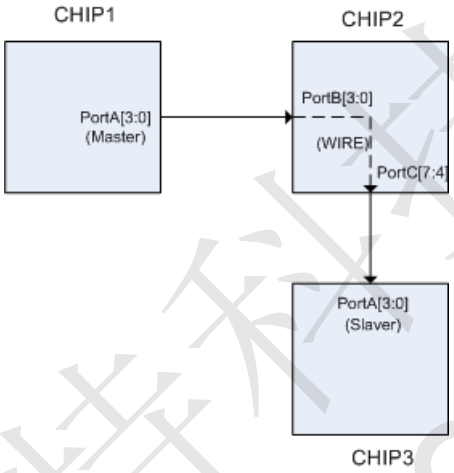


Figure 7.7 The connecting diagram of CPU array

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.4 24-Hours / One day Real-Time Clock

7.3.4.1 Features

- Time: Hours, Minutes, Seconds and Half second
- 24-Hours / One day
- Optimized for Low-Power Operation
- Clock Source: External Crystal 32768 Hz (Enable the 32768 Crystal Output at IDE tools option)
  or LP32K(32768Hz ± 2%) (Enable the Low Power 32K Output at IDE tools option)

Note: LP32K could be not precise at low/high voltage case . If user need a precise clock for application, user must choose External Crystal 32768Hz as clock source of 24-Hours real-time clock.

7.3.4.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
CLOCK_CTL.L	0AH	00	W	0	0	0	0	0	0	0	GO	Control Register Low Byte
CLOCK_CTL.H	0AH	00	W	0	0	0	0	set_halfsecond_time	set_second_time	set_minute_time	set_hour_time	Control Register High Byte

GO: 1-> Clock Counting, 0-> Clock Stop

Set_hour_time: Setting the hour value

Set_minute_time: Setting the minute value

Set_second_time: Setting the second value

Set_halfsecond_time: Setting the half-second value

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
CLOCK_DAT1	0BH	00	W	Write_DATA_Buffer[15:0]								Write Data1 Value
CLOCK_DAT1.L	0BH	00	R	0	0	Current Minute						Data1 Register Low Byte
CLOCK_DAT1.H	0BH	00	R	0	0	0	Current Hour					Data1 Register High Byte

Current Minute: Minute of current time

Current Hour: Hour of current time

OPTION	Write_DATA_Buffer[15:0]															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Set_hour_time=1	-	-	-	-	-	-	-	-	-	-	-	Hour_Time				
Set_minute_time=1	-	-	-	-	-	-	-	-	-	-	Minute_Time					
Set_second_time=1	-	-	-	-	-	-	-	-	-	-	Second_Time					
Set_halfsecond_time=1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	***(1)***

Hour_Time[4:0] : Hour Data Value of Time

Minute_Time[5:0] : Minute Data Value of Time

Second_Time[5:0] : Second Data Value of Time

(1) : Half-Second Data Value of Time

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
CLOCK _DAT2.L	0CH	00	R	0	0	0	0	0	0	0	Current Half-second	Data2 Register Low Byte
CLOCK _DAT2.H	0CH	00	R	0	0	Current Second						Data2 Register High Byte

Current Second: Second of current time

Current Half-second: Half second of current time

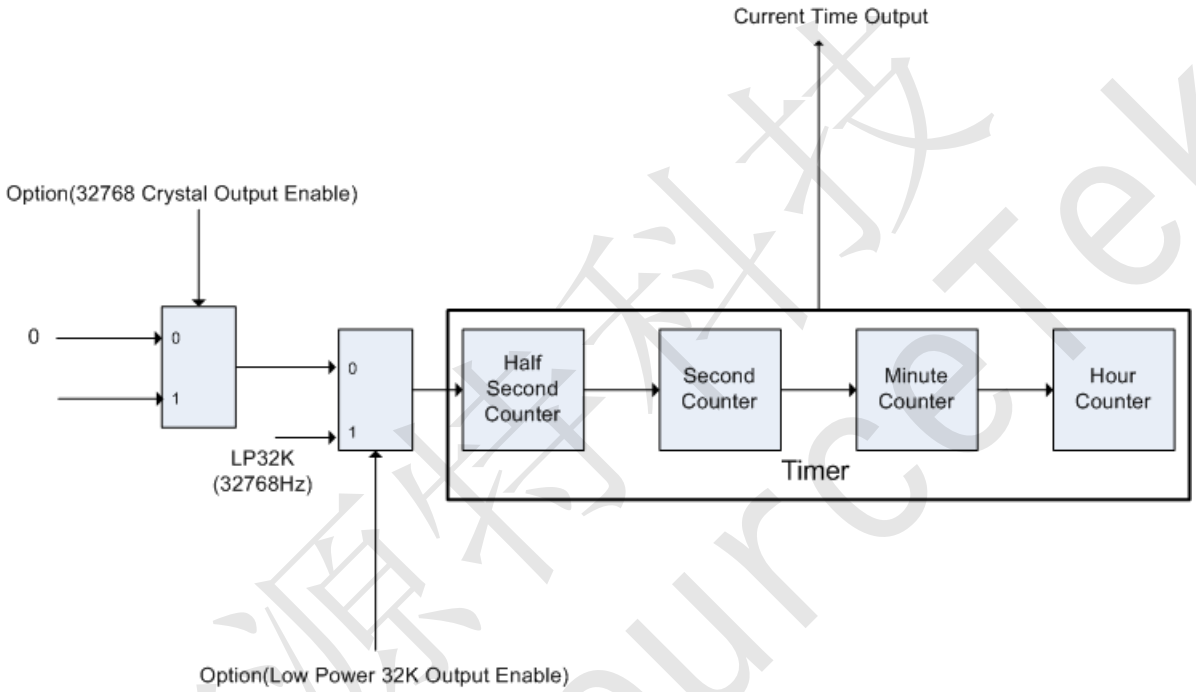


Figure 7.8 24-Hours Real-Time Clock Structure Diagram

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.5 High Speed 8channel / 10 bits signed ADC

7.3.5.1 Features

- 8 external I/O input Channels
- 10-bit Signed ADC
- Up to 200K samples per second (@ACQT = 2*TAD, ADC clock = 4Mhz)
- Programmable acquisition time
- ADC start conversion by S/W, Audio PWM, Timer, RTC or External I/O pin

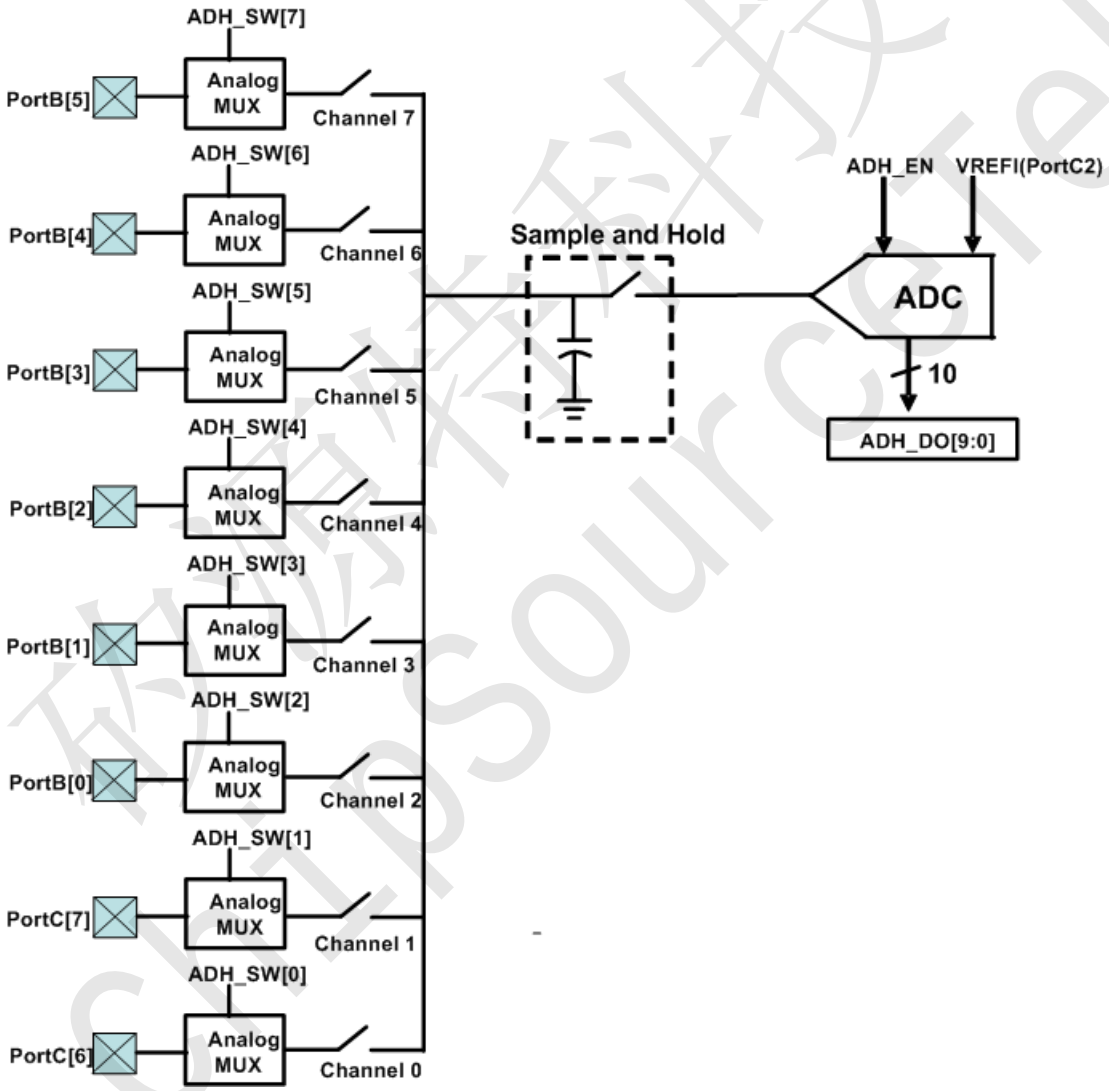


Figure 7.9 High speed 8-Channels / 10-bits ADC Structure Diagram

Note: If user need more precise ADC for application, user can use PortC2 as voltage-reference input(VREFI) of ADC. Independent voltage-reference input pin can improve ADC precision.

Note: Enable ADC verf input at option, PortC2 is as ADC voltage-reference input(VREFI), not as I/O pin.

*** The decouple capacitor (10uF) must be as near as possible to VCC and VSS.*

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.5.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG0.L	40H	00	R/W	-	-	ACQT[1:0]		-	ADCS[2:0]			High Speed 10-bit ADC control0
ADL_CFG0.H	40H	00	R/W	ADH_EN	-	-	-	-	TRGSRC [2:0]			

ADH_EN: High speed 10-bit signed ADC enable bit

ADCS[2:0]: High speed ADC clock select bit

000 = 512K 001 = 1M 010 = 2M 011 = 4M others = N/A

TRGSRC[2:0] : Select trigger source

000 = software trigger 001 = Audio PWM 010 = Timer1 011 = Timer2

100 = RTC Timer 101 = PortC[6] 11X = PortB[0]

ACQT[1:0] : A/D acquisition time select bits

00 = 2 TAD 01 = 4 TAD(default) 10 = 8 TAD 11 = 16 TAD

Note: If ADH_EN is not set to high, ADH_CFG1 can not be written.

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_CFG1.L	41H	00	R/W	ADH_SW[7:0]								High Speed 10-bit ADC control1
ADL_CFG1.H	41H	00	R/W	SWTRG	ADH_SW[14:8]							

SWTRG : Software Trigger

1 = Setting this bit starts the A/D conversion cycle.

This bit is automatically cleared by hardware when A/D conversion has completed.

0 = A/D conversion is completed

ADH_SW[14:0] : These PortB[5:0] and PortC[7:6] pins associated with the 10-bit A/D Converter can individually be configured as an analog input or digital I/O using the ADH_SW[7:0] registers.

ADH_SW[14]: 1 = VDD (LDO 1.6V)

ADH_SW[13]: 1 = VSS (Chip Ground)

ADH_SW[12]: 1 = VCC (Chip Power)

ADH_SW[11]: 1 = Temperature (TEMP_EN must be enabled, See 9.5 Temperature sensor)

ADH_SW[10]: 1 = (N/A)

ADH_SW[9]: 1 = BGO (Band Gap 0.8V)

ADH_SW[8]: 1 = Microphone amplifier analog input (Refer to Sector 9.6)

ADH_SW[7]: 1 = PortB[5] is channel 7 analog input, 0 = PortB[5] is digital I/O

ADH_SW[6]: 1 = PortB[4] is channel 6 analog input, 0 = PortB[4] is digital I/O

ADH_SW[5]: 1 = PortB[3] is channel 5 analog input, 0 = PortB[3] is digital I/O

ADH_SW[4]: 1 = PortB[2] is channel 4 analog input, 0 = PortB[2] is digital I/O

ADH_SW[3]: 1 = PortB[1] is channel 3 analog input, 0 = PortB[1] is digital I/O

ADH_SW[2]: 1 = PortB[0] is channel 2 analog input, 0 = PortB[0] is digital I/O

ADH_SW[1]: 1 = PortC[7] is channel 1 analog input, 0 = PortC[7] is digital I/O

ADH_SW[0]: 1 = PortC[6] is channel 0 analog input, 0 = PortC[6] is digital I/O

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Note: If user need to enable more A/D channels than one, user should enable ADC interrupt in order to read A/D conversion data of more channels. When some one channel is converted completely, it will generate an interrupt to CPU. Every active channel is converted sequentially.

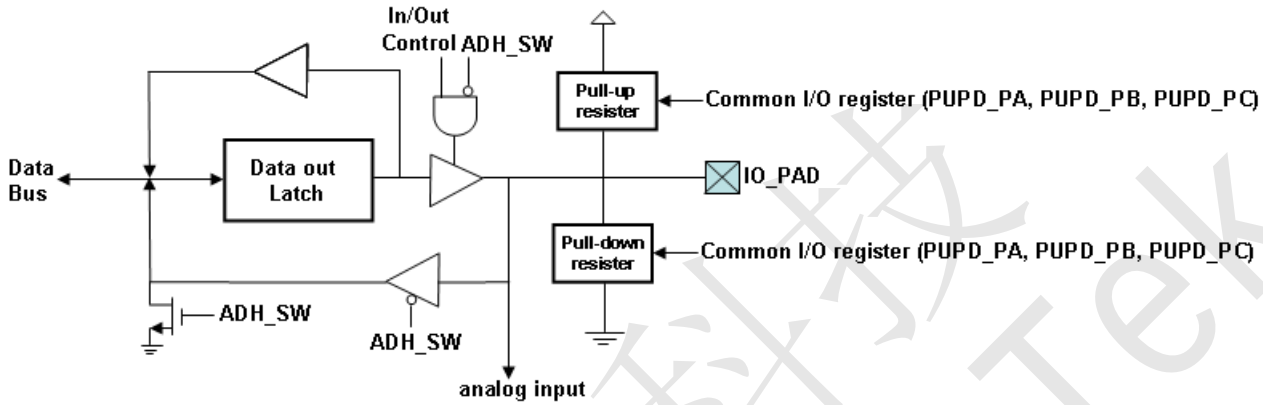


Figure 7.10 ADC External I/O Input PAD Diagram

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
ADH_DO.L	44H	00	R	ADH_DO[1:0]		0	0	0	0	0	0	High Speed 10-bit ADC result
ADL_DO.H	44H	00	R	ADH_DO[9:2]								

ADH_DO[9:0] (Only read): 10-bit Signed ADC Data Output

*** The decouple capacitor (10uF) must be as near as possible to VCC and VSS.*

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.3.6 TRA1402 Interface

In order to enable Tritan TRA1402 Audio Recording interface, user should set TRA_EN bit in the TRA_CFG register before TRA1402 controller operation.

7.3.6.1 Features

- SCLK pin can set as floating status by setting CKF bit in the TRA_CFG register
- The bit number of parallel-to-serial / serial-to-parallel converter is up to 16 for the TRA1402 write/read data.

I/O Port	TRA1402 interface	Direction	Description
PortB[2]	SYNC	O	TRA1402 32K(32000Hz) SYNC output
PortB[1]	DIO	I/O	TRA1402 data input and output
PortB[0]	SCLK	I	TRA1402 clock input

7.3.6.2 Control/Data Registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
TRA_CFG.L	46H	00	W/R	SYNC_EN	CKSEL	CKF	BitNum[4:0]					TRA1402 control register
TRA_CFG.H	46H	00	W/R	TRA_EN			TRA_INT_EN	FIFO_MODE	Auto_Polling	RCV	SEND	
TRA_DAT.L	47H	00	W/R	TRA_DAT[7:0]								TRA1402 data register
TRA_DAT.H	47H	00	W/R	TRA_DAT[15:8]								

TRA_EN: TRA1402 interface enable bit

TRA_INT_EN: TRA1402 interrupt enable

SYNC_EN: TRA1402 interface 32K(32000Hz) SYNC output enable bit

RCV:

1 = Setting this bit starts to receive data. This bit is automatically cleared by hardware when receiving data has completed.

0 = receiving data is completed

SEND:

1 = Setting this bit starts to send data. This bit is automatically cleared by hardware when sending data has completed.

0 = sending data is completed

Note: Both SEND and RCV are simultaneously set to one which is prohibited.

CKSEL: Select SCLK clock speed

0 = 8M clock speed (default)

1 = 16M clock speed

CKF:

0: the output of SCLK pin is controlled by hardware.

1: the output of SCLK pin is floating.

BitNum: bit number of sending or receiving, range from 1 to 16

TRA_DAT:

W: write transmission Left-Justified data TRA_DAT[15:0] to TRA1402.

R: Read received Left-Justified data TRA_DAT[15:0] from TRA1402

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Auto_Polling: Enable Auto-Polling mode. (See Figure 7.11)

Continuously polling tra1402 status bit **FEPT/DRDYEN** by hardware and generate interrupt when reading tra1402 status bit **FEPT/DRDYEN** is high**.**

FIFO_MODE:

1: Auto Polling tra1402 status bit **FEPT** on tra1402 FIFO mode.

0: Auto Polling tra1402 status bit **DRDYEN** on tra1402 Non-FIFO mode.

Auto_Polling	FIFO_MODE	Function Description
0	X	Disable Auto-Polling mode
1	0	Auto Polling tra1402 status bit **DRDYEN** on tra1402 Non-FIFO mode
1	1	Auto Polling tra1402 status bit **FEPT** on tra1402 FIFO mode

Note: It not necessary for generating interrupt at Auto-Polling mode that TRA_INT_EN is set to high .

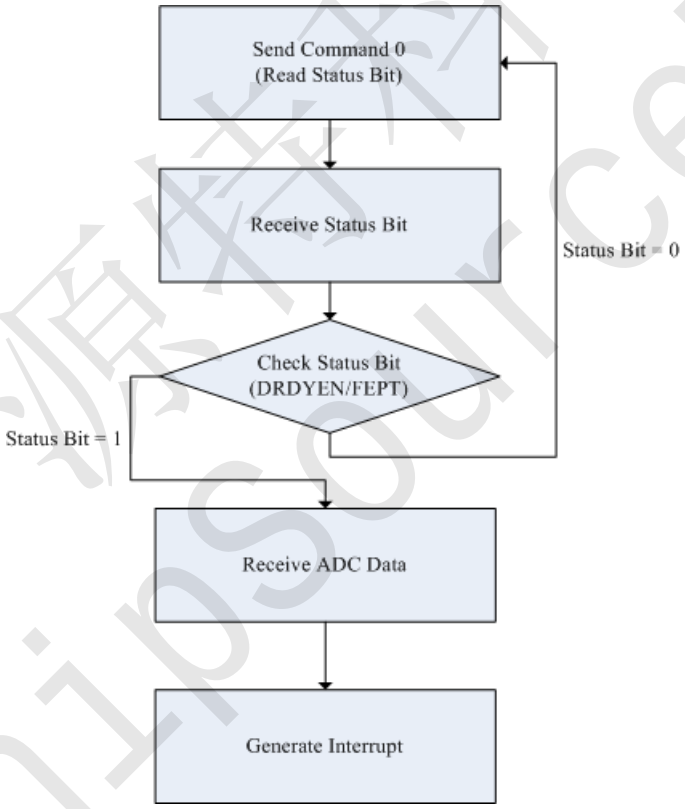


Figure 7.11 Auto-Polling Mode

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

7.4 Stereo Audio-PWM Output

Two 16-bit of digital-to-analog convert are built-in TR16F032 for stereo audio application. In order to get more output power driving, which require external amplifier for stereo output pin LCh and RCh.

Common I/O registers

Symbol	Adr	Reset	RW	b15/b7	b14/b6	B13/b5	b12/b4	b11/b3	b10/b2	b9/b1	b8/b0	Description
Audio-PWML	16H	XX	W	Audio-PWML [15:0]								Audio-PWM Audio L Channel
Audio-PWMR	17H	XX	W	Audio-PWMR [15:0]								Audio-PWM Audio R Channel

7.5 Auto-FIFO

The Auto-FIFO allows user transfer base on 4-level of data to Audio-PWM. In some case of frame base applications that data transfer is more efficient than sample base. It is advantageous to decrease number of context switch between main program and interrupt service routine (ISR). The FIFO structure reveal as below:

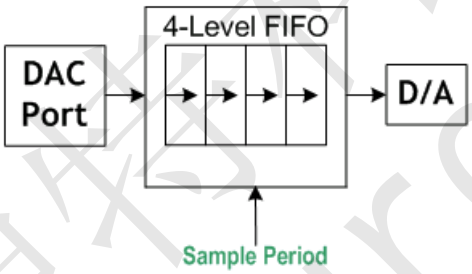


Figure 7.12 Auto FIFO Structure

An interrupt is generated when an entire 4-level FIFO is transfer completed (D\A FIFO buffer is empty), then interrupt service routine should re-load 4-level data to FIFO at ones during 32K or 64K sample period. The FIFO will automatically shift-out data to Audio-PWM at each sample period.

Note: Auto-FIFO is enable/disable by option setup.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

8. TR16F032A/B Flash Control

8.1 Flash Structure

TR16F032 is built in 32Kx16 program/data FLASH memory. This Flash is offered with sector endurance of more than 100,000(TR16F032A) / 20,000(TR16F032B) cycles, Data retention is rated at greater than 10 years. It is suited for convenient and economical updating of program, configuration, or data memory.

The sector architecture is base on sector size of 256 words/512 bytes. The sector erase operation allows the system to erase the device on a sector. The sector architecture is shown as Figure 8.1.

Sector Select(255 sectors)								Word Select(256 words)							
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Figure 8.1 The sector architecture

Note: Last sector(256th sector) is an empty sector, user can't use it. Address range of last sector is form 0xff00 to 0xffff.

8.2 Flash Sector Erase

The Sector Erase instruction needs to assign erasing sector number to AR register. When "PE = AR" instruction is executed, select of sector will be erased.

Example: Erase 16th sector (0x1000 – 0x10FF)

```
AR    = 0x0010   // assign erasing sector number
PE    = AR       // sector erasing
```

Note: Erasing time of one sector is 4.7ms.

8.3 Flash Programming

8.3.1 Word Programming

TR16F032 provide one word programming instruction. The Word Programming instruction needs to assign programming data to AR register and assign programming address to P0/P1 register. When "PM[P0/P1] = AR" instruction is executed, select of flash address will be programmed.

Example: Program 16th word address (0x0010)

```
P0 = 0x0010        // assign programming address
AR  = 0x5678       // assign programming data
PM[P0] = AR        // word programming
```

Note: Programming time of one word is 37us.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

8.3.2 Sector Programming by DMA

TR16F032 provide one sector programming by DMA. The Sector Programming by DMA needs to assign programming data to SRAM and assign programming sector number to AR register. When “PP = AR” instruction is executed, select of sector will be programmed

Example: Program 16th sector (0x1000 – 0x10FF)

```
AR  = 0x0040   // assign SRAM start address of programming data to AR
SA  = AR       // write in SRAM start address
AR  = 0x0010   // assign programming sector number
PP  = AR       // sector programming
```

Note: Programming time of one sector is 4ms.

8.4 Flash Read

8.4.1 Word Read

TR16F032 provide word read instruction. The Word Read instruction needs to assign reading address to P0/P1 register. When “AR = PM[P0/P1] ” instruction is executed, select of word will be read out to AR register.

Example: Read 16th word address (0x0010)

```
P0 = 0x0010      // assign reading address
AR = PM[P0]      // read word data
```

Note: Readng time of one word is two cycle of System Clock.

8.4.2 Sector Read by DMA

TR16F032 provide one sector read by DMA. The Sector Read by DMA needs to assign read sector number to AR register. When “PR = AR” instruction is executed, select of sector will be read to SRAM

Example: Read 16th sector (0x1000 – 0x10FF)

```
AR  = 0x0040   // assign SRAM start address of read data to AR
SA  = AR       // write in SRAM start address
AR  = 0x0010   // assign read sector number
PR  = AR       // sector read
```

Note: Read time of one sector is 145us.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

9. TR16F032A/B Others

9.1 Low Power Instruction

Low power instruction is used to reduce power consumption at the short time idle. For example, program is waiting a trigger (external I/O key input) at main loop of polling trigger. User can insert low power instruction into main loop of polling trigger in order to reduce power consumption. Low power instruction can reduce half power consumption of normal running (no insert low power instruction).

Low power instruction can stall CPU the cycle number of user define. During stall CPU, once interrupt or wakeup is happened, CPU will exit stall mode immediately.

Example: CPU will stall 256 cycles.

```
SPEEP    EQU   66H

         ar = 0x00ff;
         io[SLEEP]   = ar;
```

9.2 Dynamic System Clock

Operation frequency can be adjusted by software dynamically. User can adjust operation frequency in order to reduce power consumption.

Write Data	CPU Operation frequency
0	1 MHz
1	2 MHz
2	4 MHz
3	6 MHz
4	8 MHz
5	16 MHz

Example: Change CPU Operation frequency to 2MHz.

```
SPEEP    EQU   67H

         ar = 0x0001;
         io[SPEED]   = ar;
```

9.3 Spread Spectrum Clocking (SSC)

TR16F032 provide software algorithm with SSC hardware to reduce CHIP EMI. This function can reduce EMI by dynamically adjusting frequency.

Note: Please see Tritan Macro Liberary for reference.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

9.4 ICE Data RAM Monitor

ICE support Data RAM Monitor for motor control debug. SRAM content can be real-time monitoring by Data RAM Monitor. User can use Data RAM Monitor to monitor slowly varying parameter of control algorithm. Address of monitor can be assigned by user.

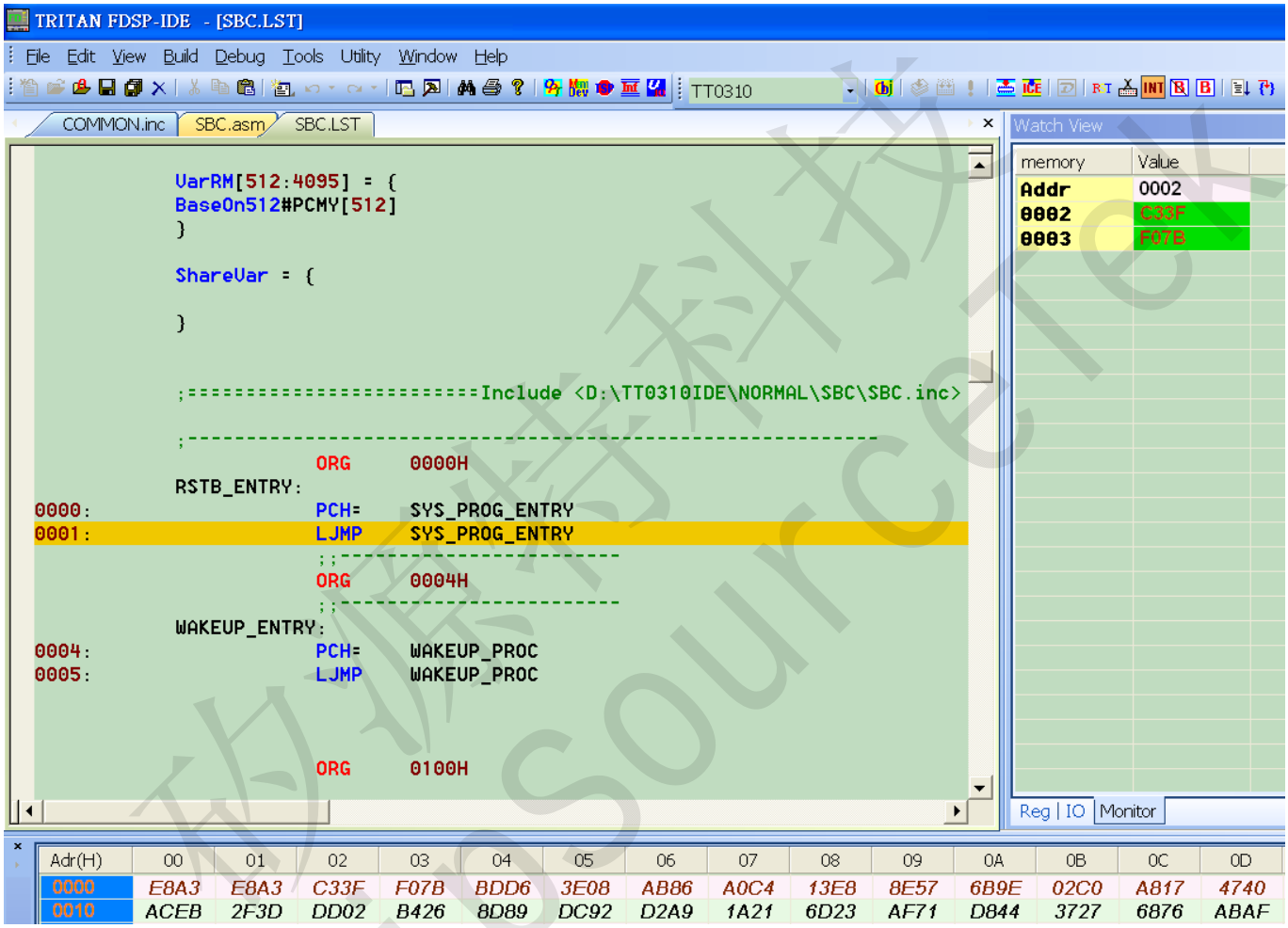


Figure 9.1 IDE operating window of ICE RAM Monitor

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

9.5 Temperature Sensor

Temperature sensor is providing a voltage that is inverse ratio as temperature. It must set **TEMP_EN** = 1 (See 9.7 microphone, MIC b12 =1) for enable the sensor reference voltage and set ADH_SW[11] = 1 for ADC input. User can refer to temperature macro.

** (Temp. sensor - 1.7mV = temp + 1℃).

**Temp. ADC data is on flash address 0x10003(Temp._ADC) at VCC=4V and temp. = 35℃

9.6 Low battery detector

Low battery detector is used to detect the “Vlbd” by a 0.8V bandgap reference. It must set ADH_SW[9] = 1 and start the ADC to read the 0.8V bandgap reference. User can refer to LVD macro.

The accuracy of low battery detector about ±5 0mV in typical

9.7 Microphone

Symbol	Adr	Reset	RW	B15/b7	b14/b6	b13/b5	b12/b4	B11/b3	B10/b2	b9/b1	b8/b0	Description
MIC.L	64H	30	R/W	-	-	**PGA[5:0]**						Microphone & Temperature Sensor
MIC.H	64H	00	R/W	-	-	-	**TEMP_EN**	-	-	-	**MIC_EN**	

***MIC_EN** : Microphone Enable *__TEMP_EN__ : Temperature Sensor Enable

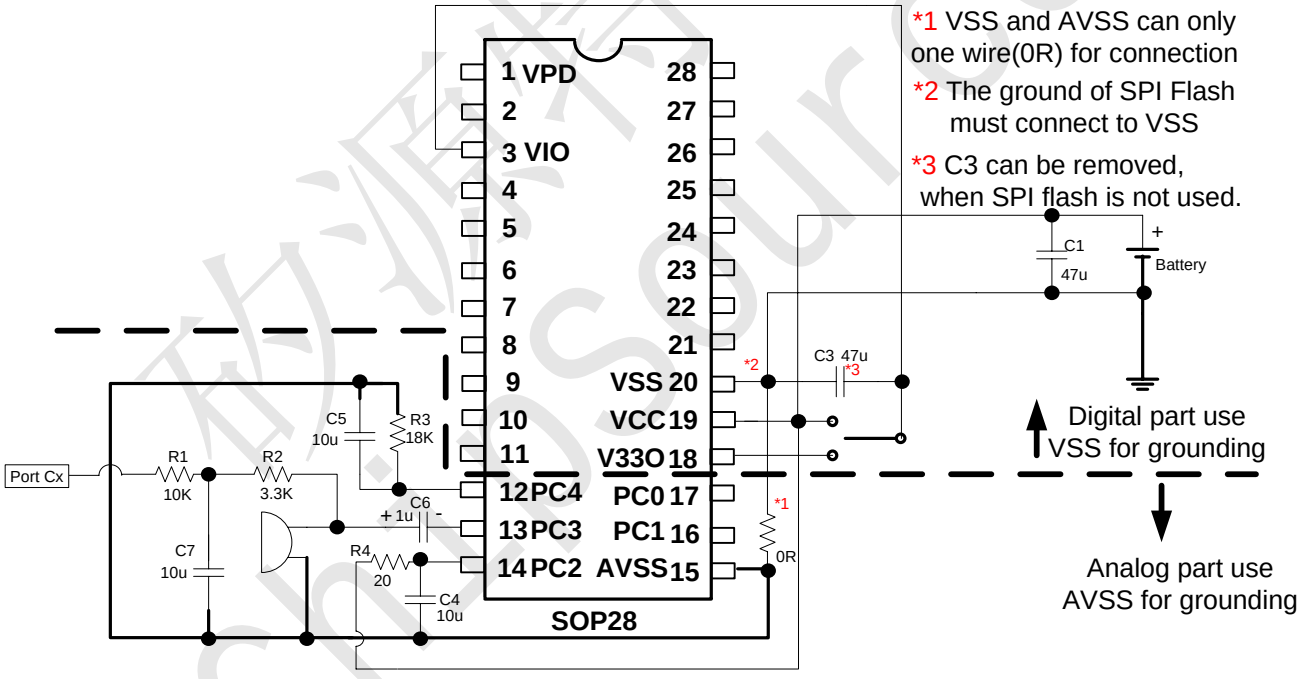


Fig 9.2 Microphone recorder application circuit (Standard version)

Note : User can use PC2(Enable the option of ADC vref input) as voltage-reference input(VREFI) of ADC for microphone application.

Note: PC3 is microphone pre-amplifier input

Note: PC4 is the bias(VMID) for microphone pre-amplifier

Note: The microphone circuit is only for microphone signal (small signal), can’t support line in signal (large signal).

Note: Port Cx must be set to low at sleep mode in order to save power.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

The optimum version (Fig 9.3) is used in the design. The voltage of PC4 must be checked for different microphone impedance, it must be below (1/2 VCC-0.1V) at highest operating voltage that can adjust by R2 (2.2K ~ 10K).

R-option (parallel with microphone) can help to adjust PC4 voltage below (1/2 VCC-0.1V), when R2 adjustment can't do it.

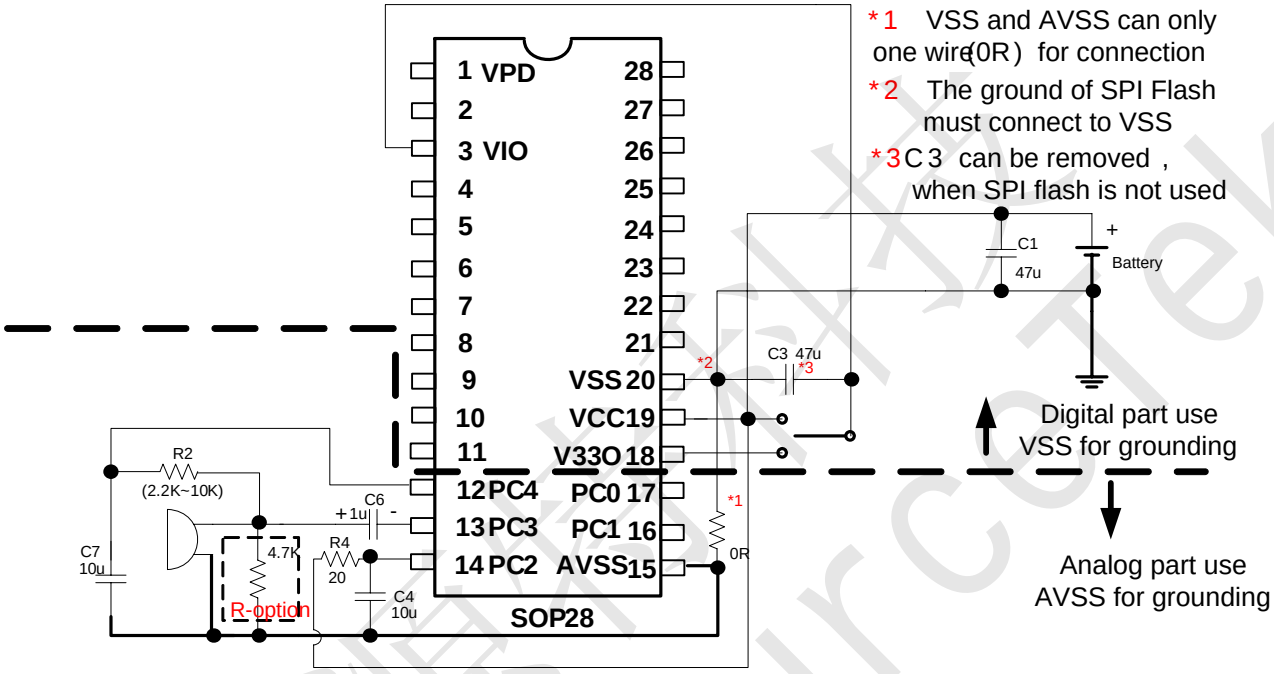


Fig 9.3 Microphone recorder application circuit (Optimum version)

There is a programmable gain amplifier (PGA) in the microphone circuit. Default gain is 37db, (PGA [5:0] = 30h). Each gain step is 1db. Maximum gain is 52db, minimum gain is -11db.PGA Input resistance is ~ 2Kohm.

PGA output is connected to ADC input (ADH_SW [8]).

User must use PortC2(Enable the option of ADC vref input) as voltage-reference input(VREFI) of ADC for microphone application.

The microphone circuit is only for microphone signal (small signal), can't support line in signal (large signal).

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

10. TR16F032A/B System Control

10.1 Halt Mode & Wake up

TR16F032 is changed into HALT mode (system clock stop, RTC stop by Option setup) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The RTC timer, PA0~PA5, PB0~PB5 and PC0~PC7 are supporting the wake-up MCU function when related I/O port raising/falling edge which selects by program. The program counter will be 04H when HALT instruction executed immediately; in addition, when wake up condition is occurred, MCU will release HALT state and program counter go-to next address after difference stable clock is delayed by option. During the Halt mode period, the SRAM will keep their previous data without changing.

10.2 Watch Dog Timer Reset (WDT)

Symbol	Adr	Reset	RW	b15/b7	b14/b6	b13/b5	b12/b4	B11/b3	b10/b2	b9/b1	b8/b0	Description
ClrWDT	1DH	XX	W									Clear WDT
RealT	1DH	0000	R	RealT[15:0]								Watch Dog Real-Time Counter

The watch dog timer (WDT) is used to reset whole chip when detect unexpected execution sequence of instructions caused by accident condition, avoiding dead lock of MCU program. Software shall run an "clear watch dog timer"(CLRWDT) instruction before this timer time out. It will generate a reset signal to reset whole system when WDT overflow.

WDT will be reset when wake-up from halt or after power on or software clear. In test mode, watch dog timer will be disabled no matter watch-dog-timer is time-out or not.

The reset watch dog timer code syntax is strongly recommended as: "**CLRWDT = AR**".

10.3 Low Voltage Reset

When VCC power is applied to the chip, the low voltage reset is initially enabled by default, it will be disabled when in halt mode. The internal system reset will be generated if VCC power below the voltage of LVR(option setup). The normal operation of LVR is always enable expect disable in HALT mode.

10.4 Reset System

TR16F032 reset is come from four signals which are power on reset, low voltage reset(LVR), external "RSTINB" pin and WDT overflow reset. A dedicated resetb input pin is provided to reset this chip. For normal operation of this chip, a good reset is needed. This pin has 30K ohm pull up resistor. The operation frequency of MCU will go back to BANK0 mode when reset occurred.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

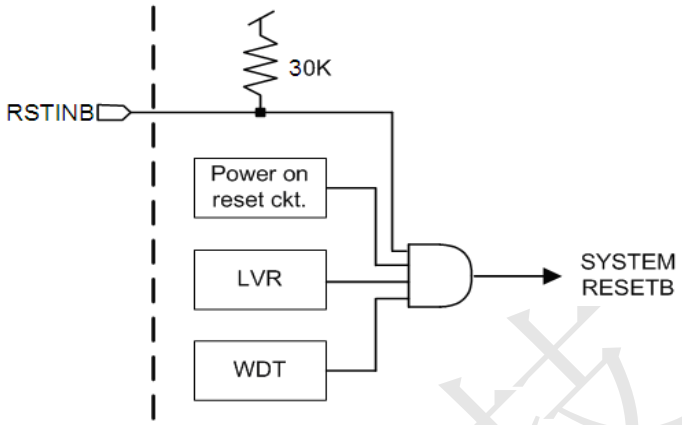


Figure 10.1 Reset system block diagram

10.5 Clock System Architecture

TR16F032 clcok system supports internal ROSC(65.536MHz) for System Clock, and External Crystal 32768Hz or Low power RC oscillator(32768Hz ± 2%) for RTC function.These crystal pins X32KI and X32KO can be shared with PortC[1], and PortC[0] respectively.

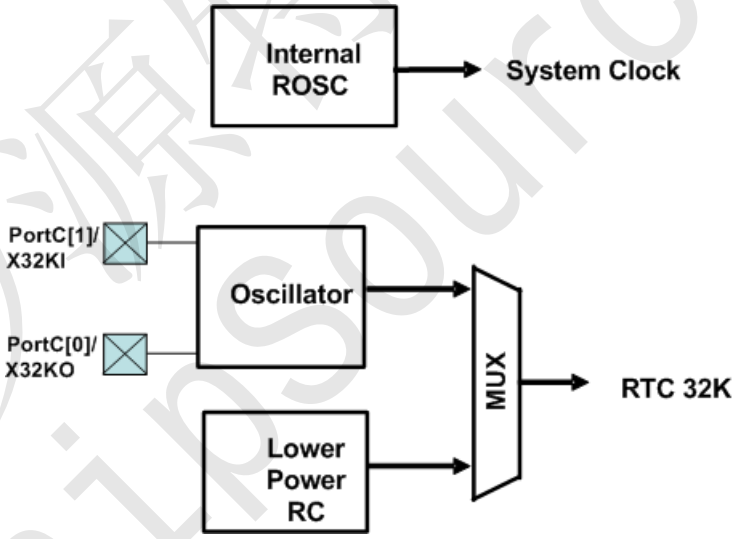


Figure 10.2 Clock System Diagram

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

11. TR16F032A/B Electrical Characteristics

11.1 Absolute Maximum Rating

Parameters	Symbol	Value	Unit
DC Supply Voltage	VCC	<5.5	V
Input Voltage	Vin	-0.5 to VCC+0.5	V
Operating Temperature Range	Ta	0 to 75	℃
Storage Temperature Range	Tstg	-50 to 150	℃

11.2 DC/AC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted

Parameters	Symbol	Minimum	Typical	Maximum	Test Condition
Operating voltage	VCC	1.8 V	-	5.5 V	
Operating frequency (BANK0)	Fbank0	1.024MHz ±1%		16.384MHz ±1%	
Operating frequency (BANK2)	Fbank2		32.768MHz ±1%		
RC oscillator frequency	Frc1		65.536MHz ±1%		
Low power RC oscillator frequency	Frc2		32768Hz ±2%		
Halt Current	Ihalt1		5uA		All function off
Operating Current	Iop		5mA		no load
input high voltage	Vih	0.8 VCC			
input low voltage	Vil			0.2 VCC	
input leakage Current	Ilk			0.1 uA	
output high voltage	Voh	0.95 VCC			no load
output low voltage	Vol			0.05 V	no load
output high current	Ioh		16 mA		Vout=VCC-0.4V, PortA, B, C, I select strength driving option
output low current	Iol		-16 mA		Vout=0.4V PortA, B, C, I select strength driving option
pull-up resistance	Rpu		100K ohm		pins with pull-up, Port A,B,C
pull-down resistance	Rpd		100K/500K ohm		pins with pull-down, Port A,B,C, I

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

11.3 10bit ADC Characteristics

(Ta = 25℃, VCC = 2.4 ~ 6V, unless otherwise noted)

Parameters	Symbol	Minimum	Typical	Maximum	Unit
ADC clock frequency	FADC			4	Mhz
Sample rate	Fsample			285	Khz
Differential Nonlinearity	DNL		±1		LSB
Integral Nonlinearity	INL		±1		LSB
Offset error	OS		±1		LSB
No Missing Code	NMC		9		Bit
Input capacitance	INC		2		pF
Input resistance	INR			37.5 *1	K

*1. Input resistance must small than 37.5K for FADC=4Mhz and TAD=2*FADC.

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

12. TR16F032A/B Application Circuit

Application Circuit 1: Stereo 16-bit PWM AMP output with Serial Flash (TYPE1)

Notice:

1. VPD VPS Decoupling Cap 47uF, please close to IC nearly.

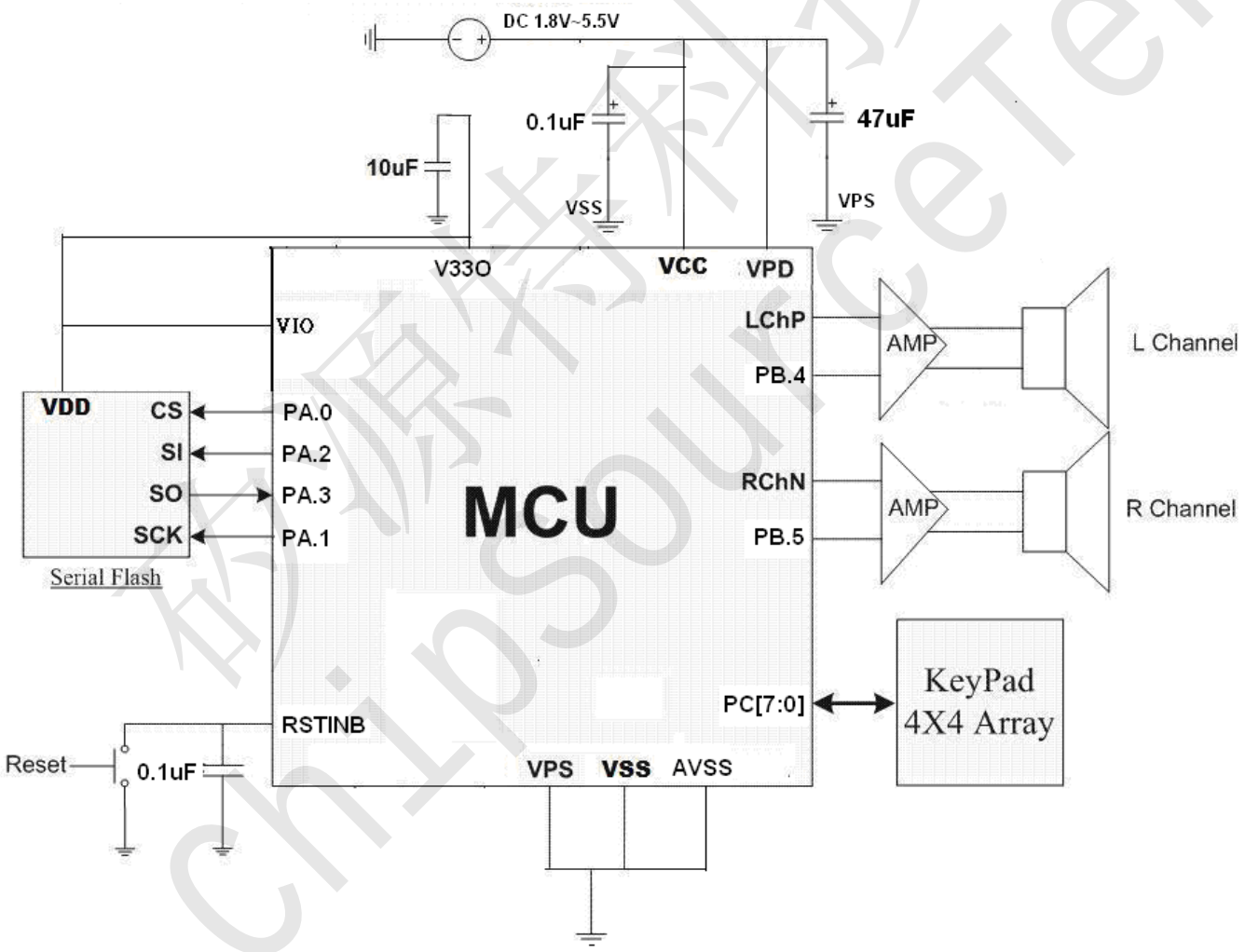
2. Power Path of VPD and VPS must pass through Decoupling Cap 47uF into IC.

3. VCC VSS Decoupling Cap 0.1uF, please close to IC nearly.

4. Power Path of VCC and VSS must pass through Decoupling Cap 0.1uF into IC.

5. VSS and AVSS are as close as possible.

6. PCB Layout about power line, Please refer to "Application Note(AN0059)"



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Application Circuit 2: Stereo 16-bit PWM AMP output with Serial Flash (TYPE2)

Notice:

1. VPD VPS Decoupling Cap 47uF, please close to IC nearly.

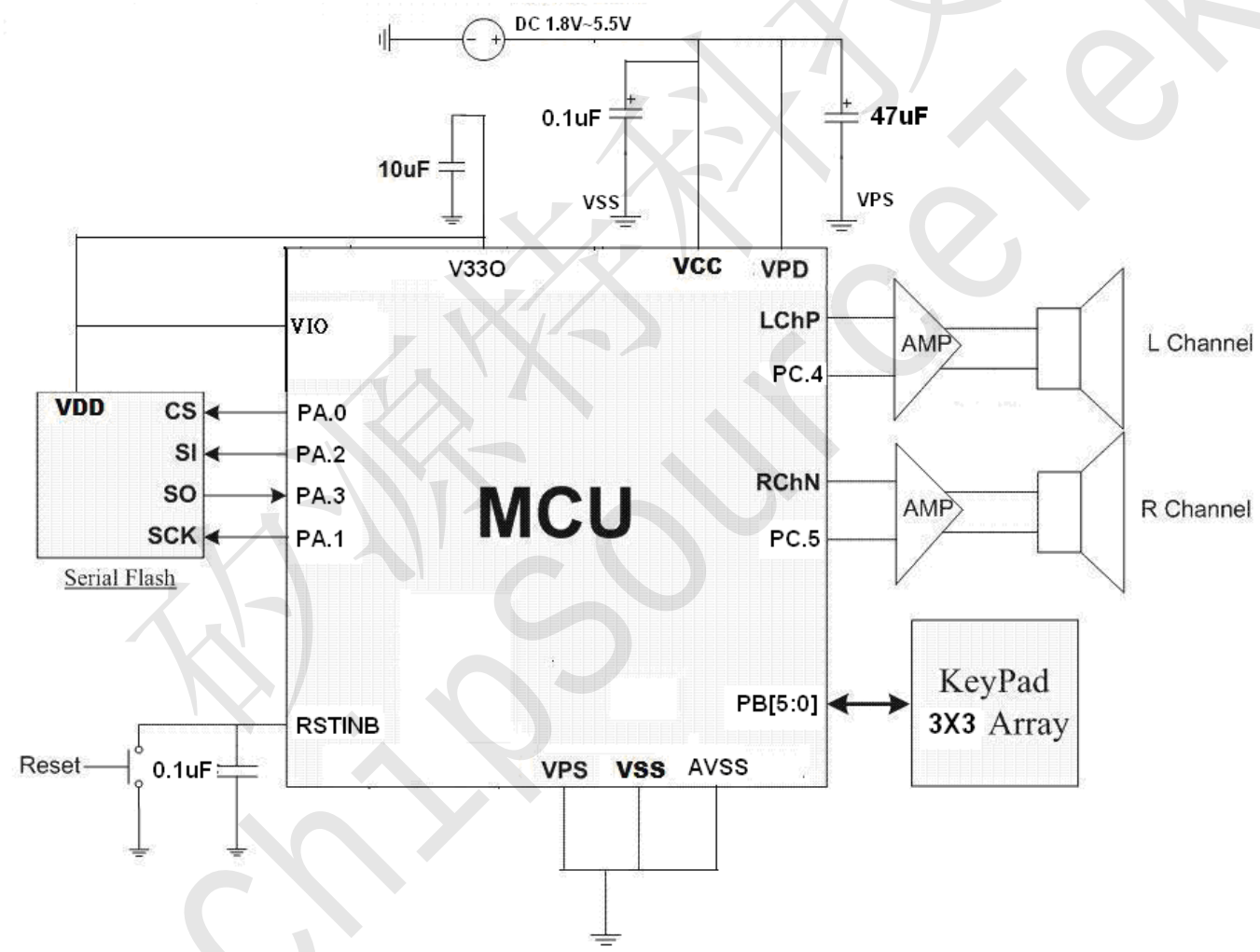
2. Power Path of VPD and VPS must pass through Decoupling Cap 47uF into IC.

3. VCC VSS Decoupling Cap 0.1uF, please close to IC nearly.

4. Power Path of VCC and VSS must pass through Decoupling Cap 0.1uF into IC.

5. VSS and AVSS are as close as possible.

6. PCB Layout about power line, Please refer to "Application Note(AN0059)"



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Application Circuit 3: Mono16-bit PWM output with Serial Flash (TYPE3)

Notice:

1. VPD VPS Decoupling Cap 47uF, please close to IC nearly.

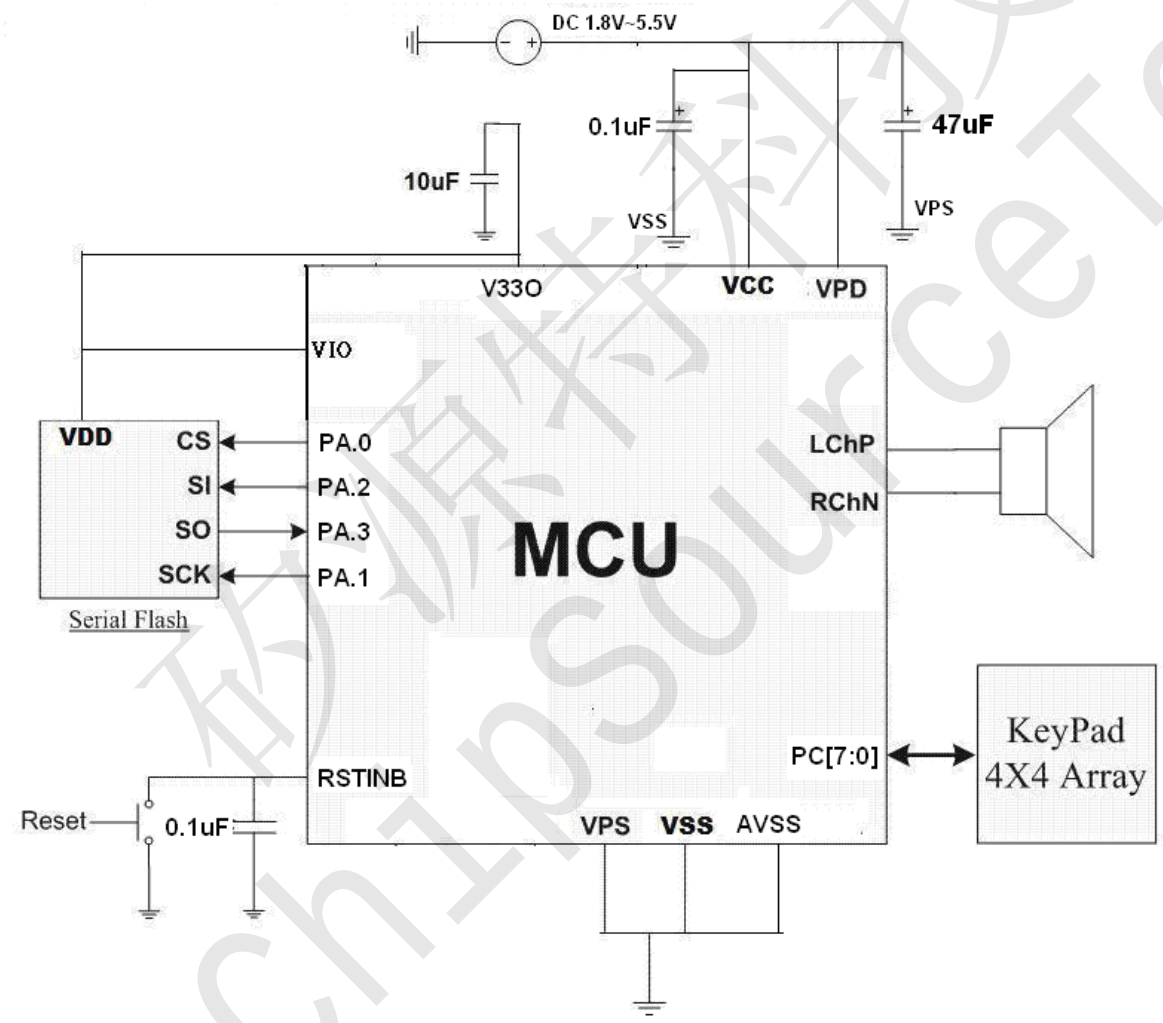
2. Power Path of VPD and VPS must pass through Decoupling Cap 47uF into IC.

3. VCC VSS Decoupling Cap 0.1uF, please close to IC nearly.

4. Power Path of VCC and VSS must pass through Decoupling Cap 0.1uF into IC.

5. VSS and AVSS are as close as possible.

6. PCB Layout about power line, Please refer to "Application Note(AN0059)"



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

13. TR16F032A/B Appendix:

Appendix 1: PORT A PIN MAP RELATE TO FUNCTION

	PORT A (I/O Power : VIO)					
	5	4	3	2	1	0
8 Ch ADC						
2 Ch Comparator						
SPI (Master)	HOLDB	WPB	SO(in)	SI(out)	CLK	CS
SPI (Slaver)						
TRA1402						
ICE						
XTAL						
PWM-Audio						
CPU Array			SO	SI	CLK	CS
Microphone						
ExtINT0						
ExtINT1						
NMI						
Timer1 EXT_Trig						
Timer2 EXT_Trig						

Appendix 2: PORT B PIN MAP RELATE TO FUNCTION

	PORT B (I/O Power : VCC)					
	5	4	3	2	1	0
8 Ch ADC	ADC Ch7	ADC Ch6	ADC Ch5	ADC Ch4	ADC Ch3	ADC Ch2
2 Ch Comparator					CAP1+	CAP1-
SPI (Master)						
SPI (Slaver)						
TRA1402				SYNC	DIO	SCLK
ICE						
XTAL						
PWM-Audio	PWM_B5 (TYPE 1)	PWM_B4 (TYPE 1)				
CPU Array			SO	SI	CLK	CS
Microphone						
ExtINT0			Trigger(0)			
ExtINT1					Trigger(1)	
NMI						Trigger(1)
Timer1 EXT_Trig				Trigger(0)		
Timer2 EXT_Trig						

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

Appendix 3: PORT C PIN MAP RELATE TO FUNCTION

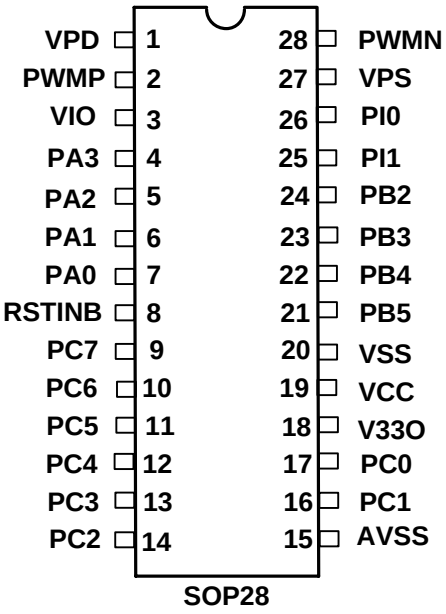
	PORT C (I/O Power : VCC)							
	7	6	5	4	3	2	1	0
8 Ch ADC	ADC Ch1	ADC Ch0				VREFI		
2 Ch Comparator	CAP2+	CAP2-						
SPI (Master)								
SPI (Slaver)	SO	SI	CLK	CS				
TRA1402								
ICE								
XTAL							X32KI	X32KO
PWM-Audio			PWM_C5 (TYPE 2)	PWM_C4 (TYPE 2)				
CPU Array	SO	SI	CLK	CS				
Microphone				VMID	MIC			
ExtINT0		Trigger(1)						
ExtINT1					Trigger(0)			
NMI						Trigger(0)		
Timer1 EXT_Trig			Trigger(1)					
Timer2 EXT_Trig	Trigger(0)			Trigger(1)				

Appendix 4: PORT I PIN MAP RELATE TO FUNCTION

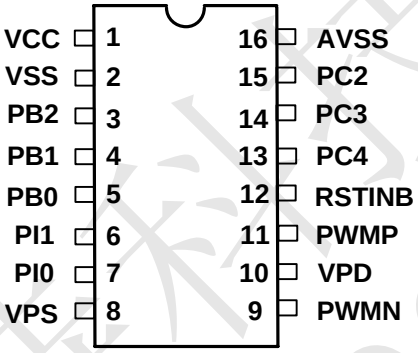
	PORT I (I/O Power : VCC)	
	1	0
8 Ch ADC		
2 Ch Comparator		
SPI (Master)		
SPI (Slaver)		
TRA1402		
ICE	ICE_SCLK(I)	ICE_SD(I/O)
XTAL		
PWM-Audio		
CPU Array		
Microphone		
ExtINT0		
ExtINT1		
NMI		
Timer1 EXT_Trig		
Timer2 EXT_Trig		

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

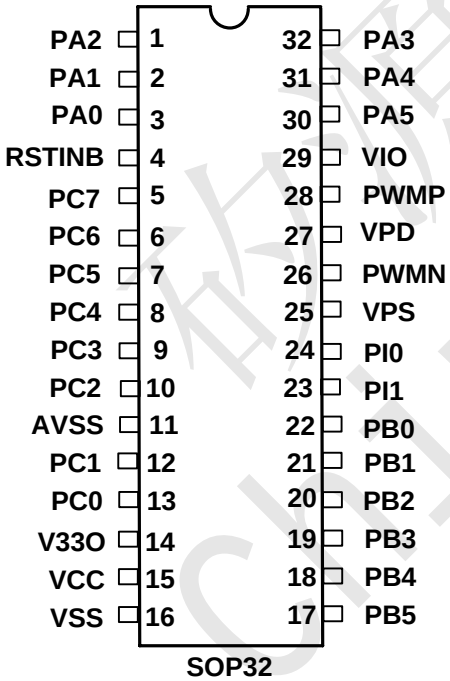
14. TR16F032A/B Package: SOP28 / SOP32 / SOP16 / LQFP32



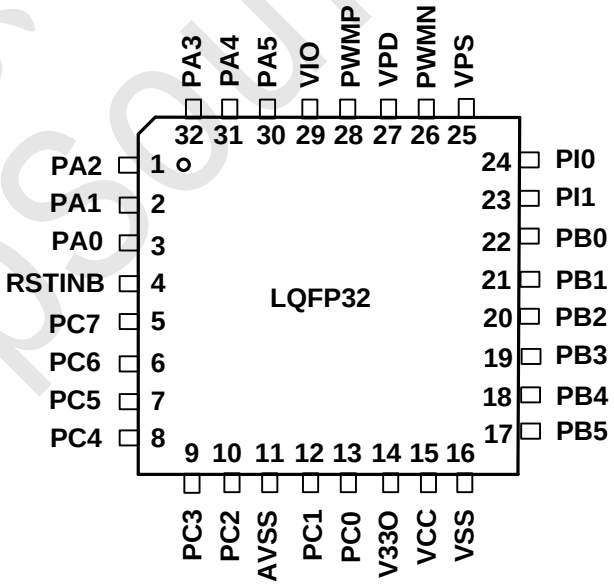
SOP28



SOP16



SOP32



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

15. TR16F032A/B Power Line PCB Layout Guide

Notice:

1. VPD VPS Decoupling Cap 47uF, please close to IC nearly.

2. Power Path of VPD and VPS must pass through Decoupling Cap 47uF into IC.

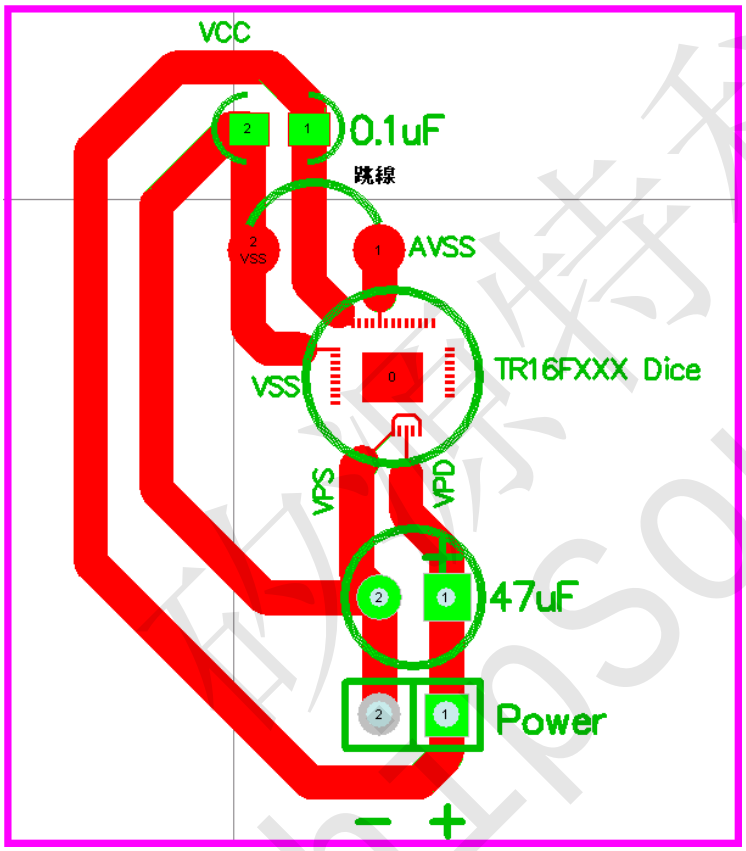
3. VCC VSS Decoupling Cap 0.1uF, please close to IC nearly.

4. Power Path of VCC and VSS must pass through Decoupling Cap 0.1uF into IC.

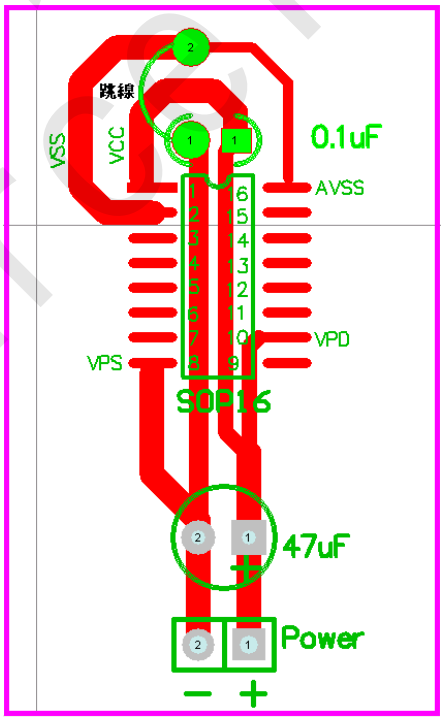
5. VSS and AVSS are as close as possible.

6. PCB Layout about power line, Please refer to "Application Note(AN0059)".

COB PCB layout Diagram:

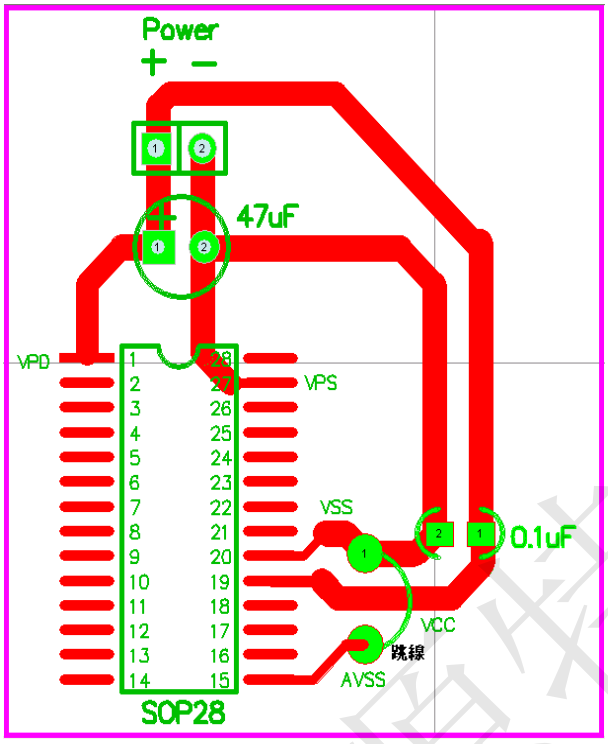


SOP16 PCB layout Diagram:

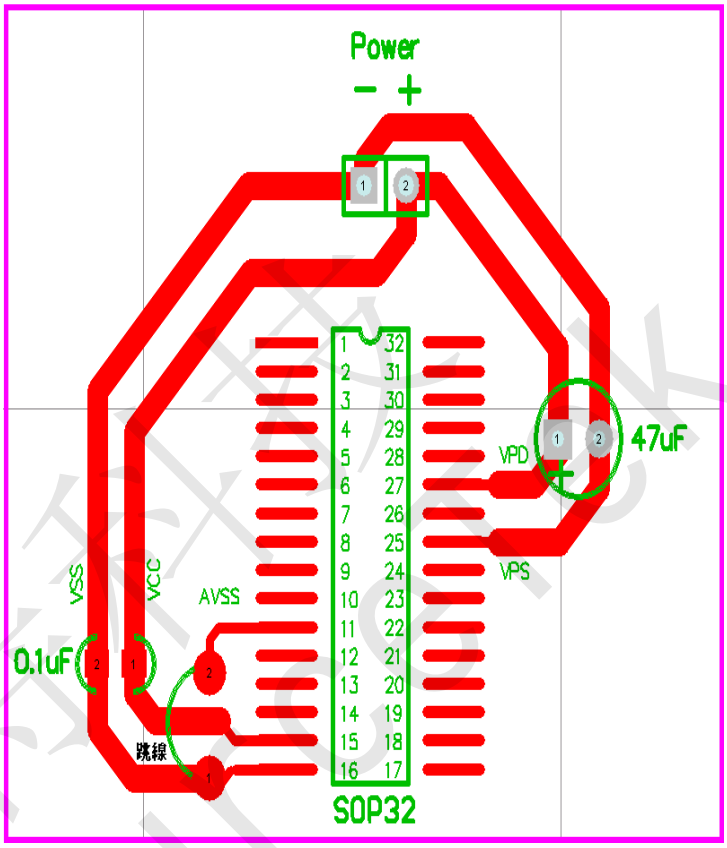


TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

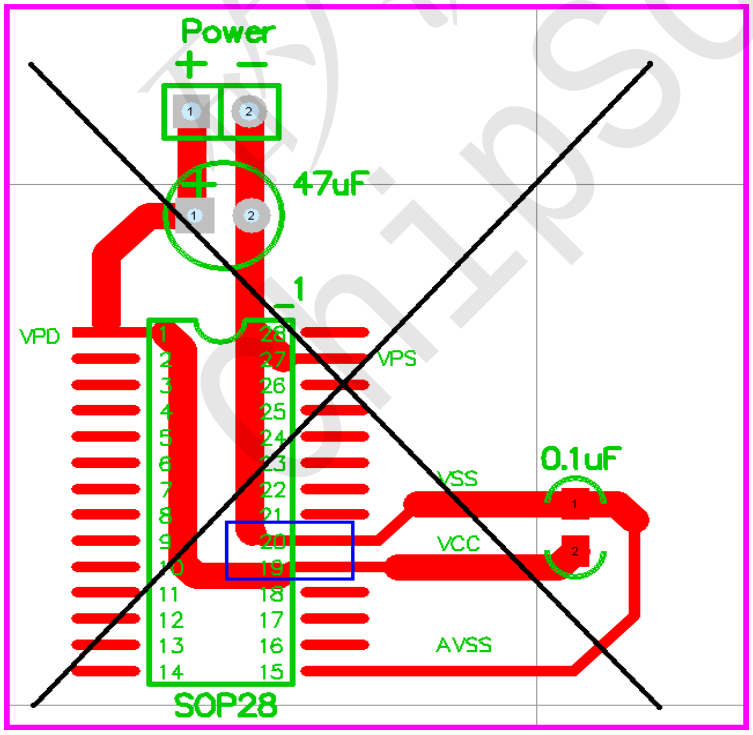
SOP28 PCB layout Diagram:



SOP32 PCB layout Diagram



Incorrect layout Diagram:



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com

16. TR16F032A/B Revision history

REVISION	DESCRIPTION	PAGE	DATE
V1.0	New establish		2013/10/1
V1.1	Modify temperature sensor parameter	45,	2013/11/25
	Add Sector 9.6	45,	
	Add Dynamic System Clock	43,	
	Modify Microphone Circuit	45,	
V1.2	Modify Microphone Circuit	45,	2013/12/27
V1.3	Modify Microphone Circuit	45,	2014/1/16
V1.4	Typical 100,000(TR16F032A) / 20,000(TR16F032B) erase/program cycles	2,	2014/4/16
V1.4	Modify Microphone Circuit	45,	2014/4/16
V1.5	Modify Package Pin Out	57,	2014/7/16
V1.6	Modify Microphone Circuit	45, 46	2014/8/21
V1.7	Modify “RealT” time base to 30.517ns(32.768MHz)	11	2014/10/23
	Add package SOP16	57	2014/10/23
	Modify Application Circuit	51, 52, 53, 54	2014/10/23
	Add Microphone description about “R-option”	46	2014/10/23
	Add Power Line PCB Layout Guide	58, 59	2014/10/23
V1.8	Modify “MODX”	12	2014/11/28
	Modify “DAC” to “Audio-PWM”	40	
	Add LQFP32 Package	57	

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Sales@ChipSourceTek.com Tony.Wang@ChipSourceTek.com