TRSP(M)4040A OTP-type Speech IC

1. TRSP(M)4040A General Descriptions

TRSP(M)4040A series are 4-bits micro-controller which could play 1 channel melody or 1 channel ADPCM with PWM direct drive circuit. PWM resolution is 8/10/12 bits. They include a low cost, high performance CMOS micro-processor. The clock frequency of this up is typically 4.096 (±3%) MHz. This chip operates over a wide voltage range of 1.5V~5.5V. It contains program ROM (PROM) and data ROM (DROM) inside. The program ROM is 4K/8K words and data ROM size is120K/112K bytes. The maximum working SRAM is (64+2) nibbles. It is provided with total 4 software programmable I/O Ports.

2. TRSP(M)4040A Features

- Operating voltage: 1.5V to 5.5V
- MCU Operation frequency: 2.048/4.096 MHz
- Memory Size
  - Program ROM size: 4K/8K*12-bits OTP type
  - Data ROM size: 120K/112K bytes OTP type
  - SRAM size: 96*4 bits
  - User register: 2*4 bits
- Wakeup function for power-down mode:
  - HALT mode wakeup source: Port A can wake up from HALT mode to NORMAL mode and executing wakeup sub-routine program.
- 4 input/output pins: Port A can be defined as input or output port bit by bit.
- Three reset condition:
  - Low voltage reset. (LVR = 1.45V)
  - Power on reset.
  - Watch dog timer overflow.
- One internal interrupt sources:
  - PWM interrupt.
- WDT
  - Watch dog timer, can enabled/disabled by option.
  - WDT period is 256*256*16/Fsys. (WDT period is 0.13 sec for system clock=2.048MHz)
- Audio output:
  - Support PWM mode.
  - Support 8/10/12 bits.
- Support option set for pull down resistor 1M, 50K Ohm, low voltage reset…etc.
- Oscillator fuse option ±3%, temperature & voltage compensation.
- Support security option (1 bit) for read inhibition.
- Support 16-levels LVD function.

3. TRSP(M)4040A Packaging and Pads Information

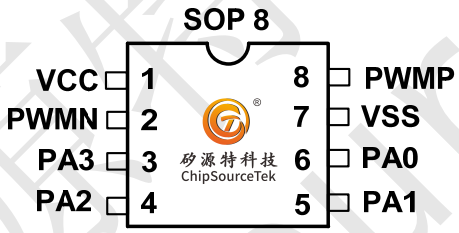
3.1 Pads

PAD Name	Type	State After Reset	Description
Reset, Power Input			
VCC	P	High	Power input.
VSS	P	Low	Ground input.
General I/O ports			
PA3~PA0	I/O	zzzz	Port A is a programmable input/output port.
Audio output pads			
PWMP	O	Low	Audio output PWM(+).
PWMN	O	Low	Audio output PWM(-).

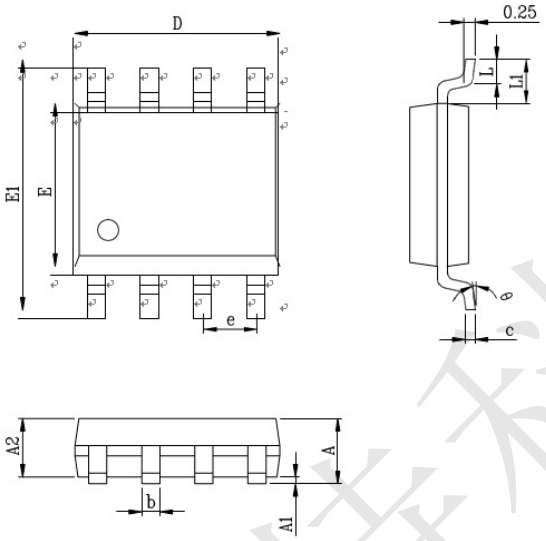
Table 1: Pad Description

3.2 Package

TRSP(M)4040A provides SOP8



3.2.1 SOP8



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.35	1.75
* A1	0.10	0.23
A2	1.30	1.50
* b	0.39	0.45
c	0.21	0.26
D	4.70	5.10
E	3.70	4.10
* E1	5.80	6.20
* e	1.24	1.30
* L	0.50	0.80
* L1	0.99	1.10
θ	0°	8°

注:1.標注"*"尺寸爲測量尺寸

3.3 Block Diagram

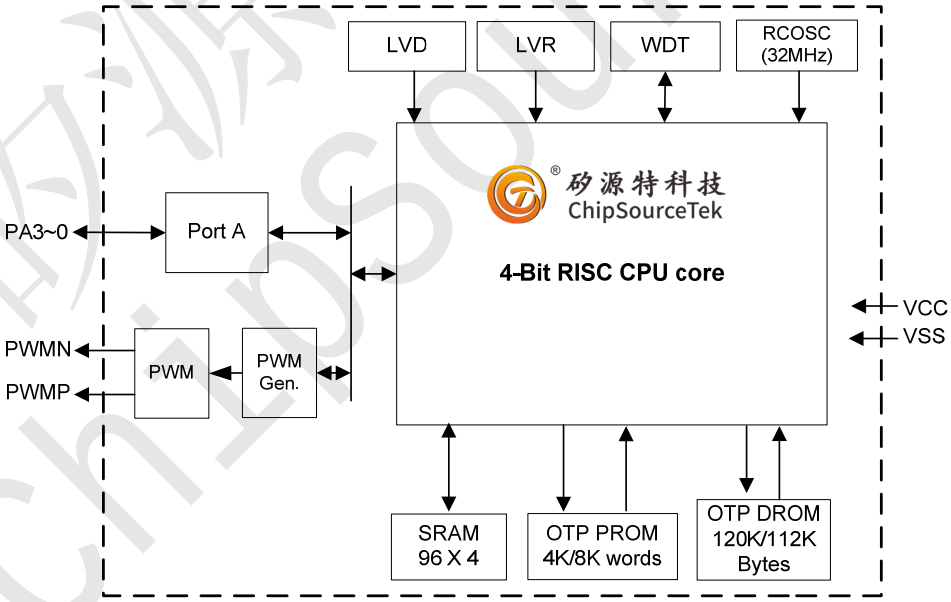


Figure 1. Block diagram

4. TRSP(M)4040A Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
DC Supply Voltage	Vcc	-0.5 to 6.0	V
Input Voltage	Vin	-0.5 to Vcc+0.5	V
Operating Temperature Range	Ta	0 to +75	℃
Storage Temperature Range	Tstg	-25 to +85	℃

Table 2: Absolute Maximum Ratings

4.2 AC Characteristics

- VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum
Operating Frequency(RC Oscillator)	Fsys1	1.987MHz	2.048MHz	2.1MHz
Operating Frequency(RC Oscillator)	Fsys2	3.973MHz	4.096MHz	4.21MHz
RC reset time-constant	Trrc	-	10 us	-
Data ROM data ready time	Tdrr	-	-	2/Fsys

- Table 3: AC Characteristics

4.3 DC Characteristics

VCC=3.0V, Ta=25℃ unless otherwise noted.

Parameters	Symbol	Minimum	Typical	Maximum	Condition
Power supply range	Vcc	1.5 V	-	5.5 V	
OTP Programming Power	Vpp	9.5 V	10 V	10.5 V	VCC = 4.8V
Supply current	Iop		1.5mA		System clock 2.048MHz PWM disabled
Stand-by Current	I_{STBY}		2.1uA		VCC=5.0V, MCU halt System clock off
Input high voltage	Vih		0.55 VCC		
Input low voltage	Vil		0.55 VCC		
Input leakage current	Ilk		0.1 uA		
Output high voltage	Voh	0.95 VCC			no load
Output low voltage	Vol			0.05 V	no load
Output high current in high source capacity mode	Ioh0		20mA		Vout=2.0 all ports High source capacity
Output low current in high sink capacity mode	Iol0		20mA		Vout=1.0 all ports High sink capacity
PWM output load		-		8 ohm	Speaker impedance
Pull-down resistance #1	Rpd1	-	50K Ohm	-	PA pins with pull-down Vin=3.0V
Pull-down resistance #3	Rpd2		1M Ohm		PA pins with pull-down Vin=3.0V
Threshold voltage of low voltage reset circuit	Vlvr		1.45V		Low voltage reset circuit can't be disabled

Table 4: DC Characteristics

5. TRSP(M)4040A Functional Description

This chapter describes the function of MCU.

5.1 Program ROM (PROM)

The PROM is an OTP (One Time Programmable) type memory. The PROM is 4K*12(0000H ~ 0FFFH) or 8K*12-bits(0000H ~ 1FFFH) which stores execution program. The last 256 location of effective PROM is reserved area, the user shall not use this area in any case. Assembler shall check user program on this limit. Hardware does not need to check this restriction.
In order to reserved unused area of PROM. These regions maybe use in the future. There is one option "OTPREV" for this purpose. If all unused area of PROM wanted to fill with "0xFFF", the option "OTPREV" on IDE tool must be enabled. Otherwise, they will fill with "0x000".

PROM=4K

PROM address	Function description
0x000 ~ 0x001	Reset
0x004 ~ 0x005	Wakeup
0x008 ~ 0x009	Interrupt
0x00A ~ 0xEFF	User code
0xF00 ~ 0xFFF	Reserve area

Table 5 Memory Map of PROM 4K

PROM=8K

PROM address	Function description
0x000 ~ 0x001	Reset
0x004 ~ 0x005	Wakeup
0x008 ~ 0x009	Interrupt
0x00A ~ 0x1EFF	User code
0x1F00 ~ 0x1FFF	Reserve area

Table 6 Memory Map of PROM 8K

5.2 Data ROM (DROM)

The DROM is an OTP (One Time Programmable) type memory. It stores the 8-bits wide data for ADPCM or melody data …etc. There are two types DROM density 112K/120K bytes shown in below table by option. The last 64 location is a reserved area. The user shall not use this area in any case. Assembler shall check user data ROM on this limit. Hardware does not need to check this restriction. If 4K PROM is selected, the maximum DROM is 120K bytes. If 8K PROM is selected, the maximum DROM is 112K bytes.

PROM=4K, DROM=120K bytes

DROM address (DMA)	Function description
0x00000 ~ 0x000FF	User area
0x00100 ~ 0x001FF	User area
0x00200 ~ 0x002FF	User area
…	…
0x1DFB0 ~ 0x1DFBF	User area (Max. size of TRSP(M)4040A)
0x1DFC0 ~ 0x1DFFF	System area, last 64 location(don't use it)

Table 7 Memory Map of DROM 120K bytes

PROM=8K, DROM=112K bytes

DROM address (DMA)	Function description
0x00000 ~ 0x000FF	User area
0x00100 ~ 0x001FF	User area
0x00200 ~ 0x002FF	User area
…	…
0x1BFB0 ~ 0x1BFBF	User area (Max. size of TRSP(M)4040A)
0x1BFC0 ~ 0x1BFFF	System area, last 64 location(don't use it)

Table 8 Memory Map of DROM 112K bytes

DROM is addressed by four registers DMA4, DMA3, DMA2, DMA1 and DMA0. After these registers are specified by software, the data need enough delay time, Tdrr in the table of "AC Characteristics". After this delay time, the data can be read from data register (DMDL & DMDH).

Ex:

```
LD      (DMA0), A
…
LD      (DMA4), A       ; Set DMA0~4
LD      A, (DMDL)       ; Read low nibble data from DROM, address as DMA4~0.
LD      A, (DMDH)       ; Read high nibble data from DROM, address as DMA4~0.
```

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data. DMA0 is lowest nibble, DMA4 is highest nibble of DROM address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.
DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Write this register means reset watch dog timer if this timer is enabled by option.
DMA4	1EH	R/W	xxxx	DMA4.3	DMA4.2	DMA4.1	DMA4.0	DMA4 is highest nibble of DROM address

Table 9 SFRs about DROM

5.3 SRAM and Special Function Register

5.3.1 SRAM

There are 96 nibbles SRAM in this chip. The SRAM and I/O memory map is divided into several pages by setting MAH register (1-bit wide). The initial value of MAH is unknown and must be defined by instructions "LDMAH" before you utilize SRAM. The extra 2 SRAM nibbles in the specifications and hardware manuals of relative mask ROM products are not SRAM in fact. They are USER1 and USER2 of SFRs.

Direct Addressing		SRAM MAP
MAH=XH	00H~1FH	SFR(special function register) register
MAH=0H	20H~3FH	USER SRAM 96x4
MAH=1H	20H~3FH	
MAH=2H	20H~3FH	

Table 10 Memory Map of SFRs

The first 32-nibble, 00H ~ 1FH, are defined as a common block. Some I/O and user register is arranged in this common block for easy data operations. The other regions, 20H~3FH, are employed as SRAM.
The user must notice that the initial content of SRAM is unknown.

5.3.2 Special Function Registers

The special function register consists of common I/O and other special register.
A special function register supports LD/ADC/SBC/OR/AND/XOR/INC/DEC/RLC/RRC/CMP/ADR operation.
Bit set/clear can only be operated on the address range from 00H to 0FH, except indirect operation is used.
The following table describes all of the SFRs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	PWFG	CF	ZF	Status Register PWFG: PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
Reserved	01H	-	xxxx	-	-	-	-	Reserved
IOC_PA	02H	R/W	0000	IOCA3	IOCA2	IOCA1	IOCA0	"1" = output, "0" = input of related PA bit.
DATA_PA	03H	R/W	xxxx	DPA3	DPA2	DPA1	DPA0	Read from Port A input port and write to output port.
Reserved	04H~ 06H	-	xxxx	-	-	-	-	Reserved
USER1	07H	R/W	xxxx	USER1.3	USER1.2	USER1.1	USER1.0	General purpose user register.
AUD_DLL	08H	W	xxxx	AUD_DLL3	AUD_DLL2	AUD_DLL1	AUD_DLL0	AUD_DLL[3:2]: The bit1~0 of 10-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. AUD_DLL[3:0]: The bit3~0 of 12-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	ENINT	ENPWM	ENPWM: "1" Enable PWM, "0" Disable PWM. ENINT: Enable global interrupt.
AUD_DL	0AH	W	xxxx	AUD_DL3	AUD_DL2	AUD_DL1	AUD_DL0	AUD_DL[3:0]: The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	AUD_DH3	AUD_DH2	AUD_DH1	AUD_DH0	AUD_DH[3:0]: The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, "0" means positive.
Reserved	0CH~ 0EH	-	xxxx	-	-	-	-	Reserved
USER2	0FH	R/W	xxxx	USER2.3	USER2.2	USER2.1	USER2.0	General purpose user register.
Reserved	10H							
CNTI	11H	R/W	0000	0	SCHMIT	S2S	0	S2S: PWM input Data format 1: 2's format 0: sign SCHMIT: PA0~PA3 Schmitt trigger input SCHMIT=0 disable Schmitt trigger input (default) SCHMIT=1 enable Schmitt trigger input
Reserved	12h~ 17H	-	xxxx	-	-	-	-	Reserved
DMA0	18H	R/W	xxxx	DMA0.3	DMA0.2	DMA0.1	DMA0.0	DMA0~3, four register built a 16-bits addressing space for read DROM 8-bits data, DMA0 is lowest nibble, DMA4 is highest nibble of DROM address.
DMA1	19H	R/W	xxxx	DMA1.3	DMA1.2	DMA1.1	DMA1.0	
DMA2	1AH	R/W	xxxx	DMA2.3	DMA2.2	DMA2.1	DMA2.0	
DMA3	1BH	R/W	xxxx	DMA3.3	DMA3.2	DMA3.1	DMA3.0	
DMDL	1CH	R/W	xxxx	DMDL.3	DMDL.2	DMDL.1	DMDL.0	Low nibble of DROM data read from this address.

DMDH	1DH	R/W	xxxx	DMDH.3	DMDH.2	DMDH.1	DMDH.0	High nibble of DROM data read from this address. Writing this register means reset watch dog timer if this timer is enabled by option.
DMA4	1EH	R/W	xxxx	DMA4.3	DMA4.2	DMA4.1	DMA4.0	DMA4 is highest nibble of DROM address
Reserved	1FH	-	xxxx	-	-	-	-	Reserved

Table 11 All of the Special Function Registers

5.4 Interrupt Vector Address

Vector	Address
RESET	00H
WAKEUP	04H
INT	08H

Table 12 Interrupt Vectors

5.5 Interrupt Controller

There is only one interrupt entry point in this chip. Normally interrupt period is 32768Hz. It can be changed to 65536Hz by option “PWM64K”. Program will jump to address 0x008 when an interrupt occurs.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG:** PWM interrupt flag. CF: Carry flag. ZF: Zero flag.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM:** “1” Enable PWM, “0” Disable PWM. **ENINT:** Enable global interrupt.

Table 3 SFRs about Interrupt

If the global interrupt enable bit (INTEN) is high and interrupt request (PWFG=1) occurred, then interrupt will be accepted on next clock. On that instant, current (next) program counter, PCDH, MAH and C/Z will be stored in special hardware registers, and program counter will be loaded with entry address of that interrupt. All these are done in one clock. Interrupt enable bit will be cleared too. As long as program enters interrupt service, interrupt enable bit is cleared. It's no need to clear interrupt enable flag in interrupt routine. But hardware will not clear interrupt request flag (PWFG). Software is required to clear it.

When interrupt service routine is done, an RETI shall be executed. This instruction will restore stored program counter, PCDH, MAH and C/Z, will set interrupt enable bit=1 also. (Note that RETI is different from RETS.) Interrupt request can be accepted only when enable bit be set. Note that only one level of INT routine can be used.

5.6 Clock Operation

There are two operation modes in this chip. The state diagram of three MCU operation modes is shown below:

1. NORMAL Mode: In normal mode, system clock oscillator is running, and MCU clock source is come from main oscillator. In NORMAL mode, MCU will go to halt mode after HALT instruction executed.

2. HALT Mode: In HALT mode, the MCU clock stops, users can’t change the operation mode when in halt mode. It will go back to NORMAL mode (Program counter=0x004) when I/O wake up or reset occurred. Please refer to the section of” Halt Mode & Wakeup” for the detailed HALT mode description.

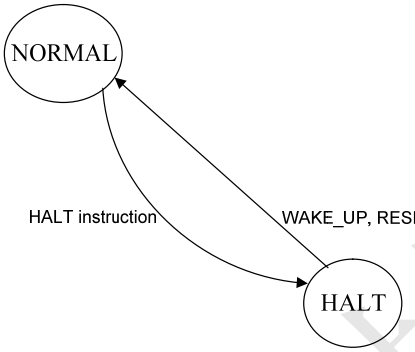


Figure 2: Clock Operation Mode

5.7 Halt Mode & Wakeup

The MCU is changed into HALT mode (program counter and system clock stop) when HALT instruction executed. It provides a power saving mode for those applications requiring a very low stand-by current. The PA[3:0] are supporting the wakeup function when rising edge occurred.

The program counter will be 0x004 when HALT instruction executed immediately, then program counter will go to next address after 64 stable clock(system clock) when wakeup condition occurred. Reset signal will release HALT state and execute reset procedure because reset is first priority when in HALT mode, so program counter will from 0x004 to 0x000, program counter goes to next address after 64 stable clock cycles. Furthermore, the SRAM will keep their previous data without changing in this mode.

5.8 Watch Dog Timer Reset (WDT)

The **Watch Dog Timer (WDT)** is used to reset whole chip when detect unexpected execution sequence caused by accident condition, avoiding dead lock of MCU program. WDT will be reset when wake up from halt, after reset or software clears it. The watch dog timer is a simple counter. It has a fixed length of **256*256*16/system-clock (ex: 0.13 sec for 2.048MHz system clock)** after the clearance of watch dog.

Software must run a "clear watch dog timer" (write to DMDH) instruction before this timer time out when WDT enabled. It will generate a reset signal to reset whole system when WDT over flow. Assembler will check user program about the "reset watch dog" instructions. If more than one "reset watch dog" is found in program, assembler will generate a warning (program code will still be generated). "HALT" instruction will reset watch dog timer. The reset watch dog timer sequence is strongly recommended as:

```
WATCHDOG:
        LD      (1DH), A
```

5.9 8/10/12 Bits PWM

There are three optional PWM output resolutions. One is 8-bits output, the sec. is 10-bits output, and the other is 12-bits output. The highest of input data is signed bit: ‘0’ represents positive, ‘1’ represents negative.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
STATUS	00H	R/W	00xx	reserved	**PWFG**	CF	ZF	Status Register **PWFG:** PWM interrupt flag.

								CF: Carry flag. ZF: Zero flag.
AUD_DLL	08H	W	xxxx	**AUD_DLL3**	**AUD_DLL2**	**AUD_DLL1**	**AUD_DLL0**	**AUD_DLL[3:2]:** The bit1~0 of 10-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 10-bits PWM if option PWM10 is 1 and PWM12 is 0. **AUD_DLL[3:0]:** The bit3~0 of 12-bits PWM, combine with AUD_DL[3:0], AUD_DH[3:0] to built 12-bits PWM if option PWM12 is 1.
PWM_CTRL	09H	R/W	--x0	reserved	reserved	**ENINT**	**ENPWM**	**ENPWM:** "1" Enable PWM, "0" Disable PWM. **ENINT:** Enable global interrupt.
AUD_DL	0AH	W	xxxx	**AUD_DL3**	**AUD_DL2**	**AUD_DL1**	**AUD_DL0**	**AUD_DL[3:0]:** The low nibble of 8-bits PWM. The bit5~2 of 10-bits PWM. The bit7~4 of 12-bits PWM.
AUD_DH	0BH	W	xxxx	**AUD_DH3**	**AUD_DH2**	**AUD_DH1**	**AUD_DH0**	**AUD_DH[3:0]:** The high nibble of 8 bits PWM. The bit9~6 of 10 bits PWM. The bit11~8 of 12 bits PWM. Note: AUD_DH3 is sign bit, "0" means positive.

Table 4 SFRs about the operation of PWM

5.9.1 8-Bits PWM

This PWM is 8-bits output resolution. An interrupt request happened when a PWM cycle completed.

The MSB of AUD_DH is signed bit, '0' for positive, '1' for negative. PWM output frequency (sample rate) is fixed at 32KHz. PWM data registers are AUD_DL, AUD_DH. The AUL_DL is low nibble (D3 ~ D0). AUD_DH is high nibble (D7 ~ D4). D7 is the signed bit and D6 ~ D0 is the length (clock number) of output active pulse. Software should write AUD_DL and AUD_DH before enable PWM.

When an interrupt request happened, PWM interrupt flag bit PWFG of STATUS register will be "1". The PWM will load previously-written-data into actual conversion port on end of a PWM code output. So program can write data into PWM data store safely at beginning of an interrupt service routine. (A PWM interrupt means PWM data loaded, next data is expected). This timing shall be controlled carefully such that data writing in the beginning of interrupt service routine is safe. If data is not changed during a conversion, previous data will be used.

This PWM output can drive 8 ohm speaker. PWM can be enabled or disabled by setting/clearing ENPWM of PWM_CTRL. When disabled, the PWMP, PWMN pins are all '0'. "HALT" instruction will disable PWM (clear ENPWM of PWM_CTRL) and the PWMP and PWMN pins will be tri-state.

5.9.2 10-Bits PWM

The frequency of PWM clock is fixed at 32 KHz if 10-bits PWM mode is selected by option. The 10-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:2]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~511. Software should write these registers before PWM is enabled. The other features of 10-bits PWM is the same as 8-bits PWM.

5.9.3 12-Bits PWM

The frequency of PWM clock is fixed at 32 KHz if 12-bits PWM mode is selected by option “PWM12S”. The 12-bits PWM data (AUD_DH[3:0], AUD_DL[3:0], AUD_DLL[3:0]) are consist of AUD_DH, AUD_DL, AUD_DLL three registers shown above. The data rage is 0 ~ 2047. Software should write these registers before PWM is enabled. The other features of 12-bits PWM is the same as 8-bits PWM.

Note: To avoid sound “Bo”, please reference application note on web site.

5.10 Reset Function

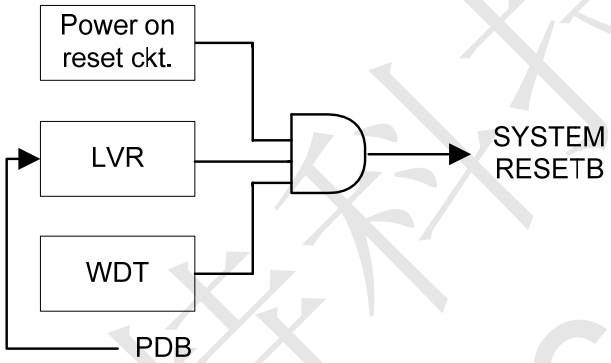


Figure 3: Reset structure

The system reset is come from three signals which are **Power on reset**, **Low voltage reset(LVR)** and **WDT overflow reset**.

For normal operation of this chip, a good reset is needed. The operation frequency of MCU will go back to normal mode when reset occurred in HALT mode.

5.11 System Clock Oscillator

This chip MCU is typically operated on 2.048MHz which is generated from internal RC oscillator 32MHz.

5.12 I/O Ports

There is one I/O port PA3~PA0, whose input/output direction are defined by IOC_PA. The wakeup functions of PA3~PA0 are enabled or disabled by option. All I/O ports provides rising or falling edge wakeup function. This double edge wakeup function can be enabled by “BIWK” option. Their 1M/50K Ohm pull down resistors are optional.

5.12.1 Port PA (input/output)

The Port A is 4-bits bidirectional I/O port. Their directions can be defined by IOC_PA bit by bit.
The following table describe the SFRs associated with Port A.

Symbol	Addr	R/W type	Reset	D3	D2	D1	D0	Description
IOC_PA	02H	R/W	0000	**IOCA3**	**IOCA2**	**IOCA1**	**IOCA0**	**“1” = output, “0” = input of related PA bit.**
DATA_PA	03H	R/W	xxxx	**DPA3**	**DPA2**	**DPA1**	**DPA0**	**Read from Port A input port and write to output port.**

Table 15: SFRs of Ports PA

In output mode, the data can be written out to external pin, and reading this output port will read the data internal latch. Pull-down resistor will be disabled when output mode is selected.
In input mode, Port A data can be read from external pin, and they are attached with 1M/50K Ohm pull-down resistor or not according to the options.

In addition, each pin of Port A also can be accompanied with wakeup function according to the options. In HALT mode, if some bits of Port A are accompanied with wakeup function, any rising edge occurred on that pin will wake up system and turn on oscillator, and the program counter of MCU will jump to the address 0x004. This device will start to execute the wakeup sub-routing.

6. TRSP(M)4040A The Application Circuit

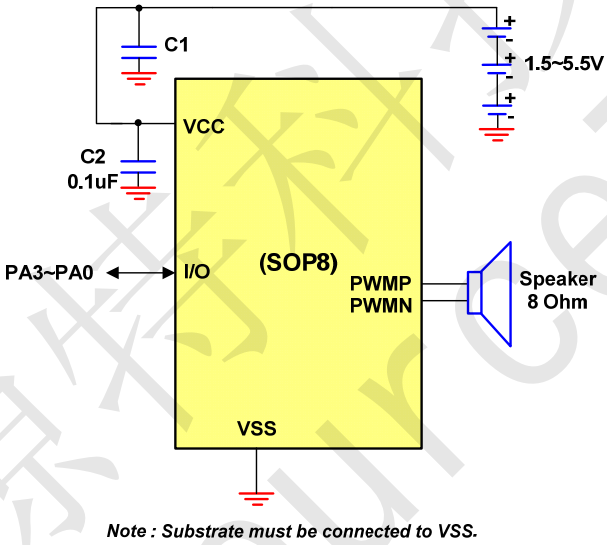


Figure 4. PWM Applications circuit

Notice: C1 : 10 uF ~ 100 uF(depends on applications), C2：0.1 uF

7. TRSP(M)4040A Option Registers table

Option Name	Function Description
WAKEBA	Wakeup enable for PA3~PA0 respectively
PD50KPA	50K Ohm pull down resistor for PA3~PA0 respectively.
PD1MPA	1M Ohm pull down resistor for PA3~PA0 respectively.
WDGENB	Watch dog timer
HALTENB	HALT mode control
PWM12S	PWM 12 bit select
PWM10S	PWM 10/8 bit select
OTPLOCK	Security control
BIWK	Bi-directional wakeup
PROM4K	PROM density selection
PROM8K	PROM density selection

Table 16 Option table

8. TRSP(M)4040A The Revision History

Version	Description	Page	Date
1.0	Established		2023-12-6

Table 17 Revision History