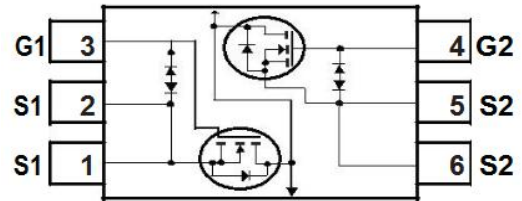




Dual N-Channel Enhancement Mode Power MOSFET

Description

The MXN2382 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected..



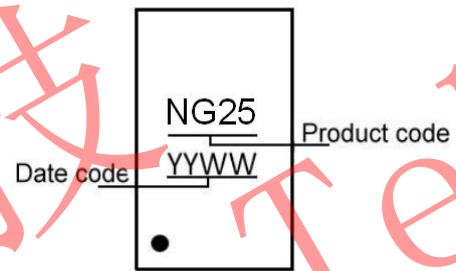
General Features

- ◆ $V_{DS} = 20V$, $I_D = 8A$
 - @ $V_{GS} = 4.5V$ $R_{DS(ON)}(Typ.) = 10m\Omega$
 - @ $V_{GS} = 4.2V$ $R_{DS(ON)}(Typ.) = 11m\Omega$
 - @ $V_{GS} = 3.8V$ $R_{DS(ON)}(Typ.) = 11.5m\Omega$
 - @ $V_{GS} = 2.5V$ $R_{DS(ON)}(Typ.) = 15m\Omega$
- ◆ ESD Rating: 2000V HBM
- ◆ High power and current handling capability
- ◆ Lead free product is acquired
- ◆ Surface mount package

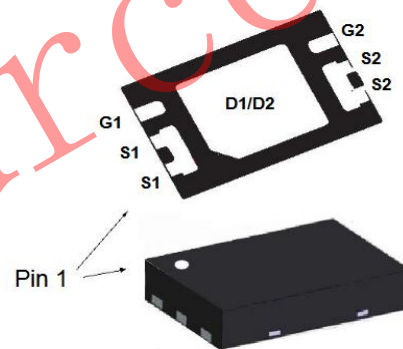
Application

- ◆ PWM applications
- ◆ Load switch

Schematic diagram



Marking Description



DFN2x3-6L Pin definition and Top / Bottom View

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	8	A
Drain Current-Pulsed (Note 1)	I_{DM}	30	A
Maximum Power Dissipation	P_D	0.98	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C



Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	20	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =20V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±10V, V _{DS} =0V	-	-	±10	μA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	0.45	0.7	0.95	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =4.5V, I _D =6A	9	10	14	mΩ
		V _{GS} =4.2V, I _D =6A	9.5	11	15	mΩ
		V _{GS} =3.8V, I _D =5.5A	10	11.5	16	mΩ
		V _{GS} =2.5V, I _D =5.5A	13	15	18	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =7A	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =10V, V _{GS} =0V, F=1.0MHz	-	1150	-	PF
Output Capacitance	C _{oss}		-	185	-	PF
Reverse Transfer Capacitance	C _{rss}		-	145	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =10V, R _L =1.35Ω V _{GS} =5V, R _{GEN} =3Ω	-	6	-	nS
Turn-on Rise Time	t _r		-	13	-	nS
Turn-Off Delay Time	t _{d(off)}		-	52	-	nS
Turn-Off Fall Time	t _f		-	16	-	nS
Total Gate Charge	Q _g	V _{DS} =10V, I _D =7A, V _{GS} =4.5V	-	15	-	nC
Gate-Source Charge	Q _{gs}		-	0.8	-	nC
Gate-Drain Charge	Q _{gd}		-	3.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =1A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	7	A

Notes:

- surface mounted on FR4 board, t≤10sec
- pulse test: pulse width≤300μs, duty≤2%
- guaranteed by design, not subject to production testing

Thermal Characteristics

Thermal Resistance junction-to ambient	R _{th JA}	126	°C/W
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

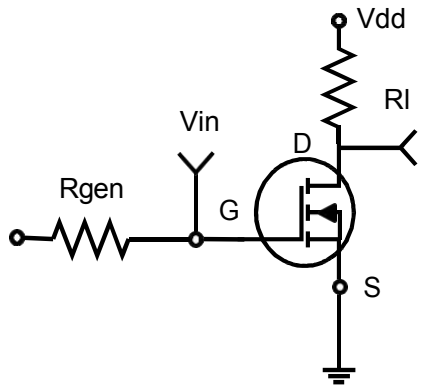


Figure 1: Switching Test Circuit

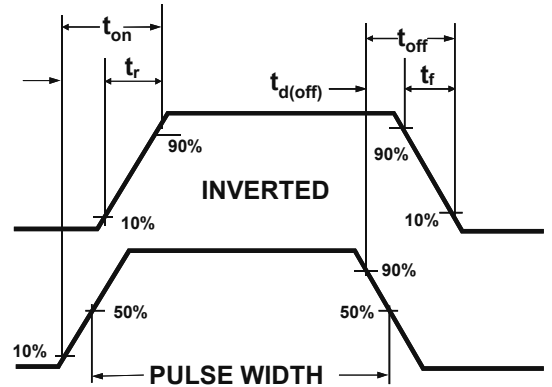


Figure 2: Switching Waveforms

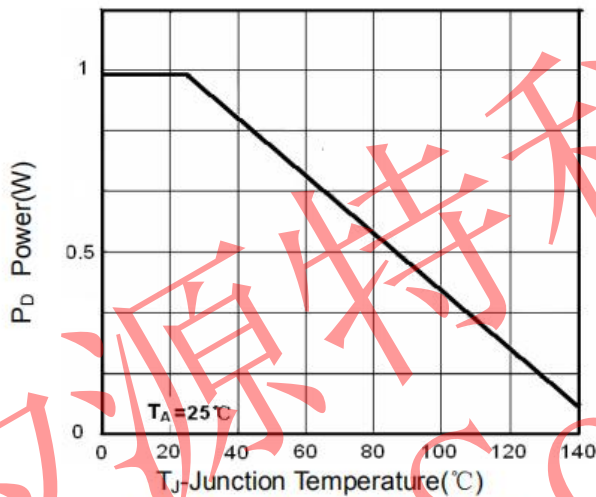


Figure 3 Power Dissipation

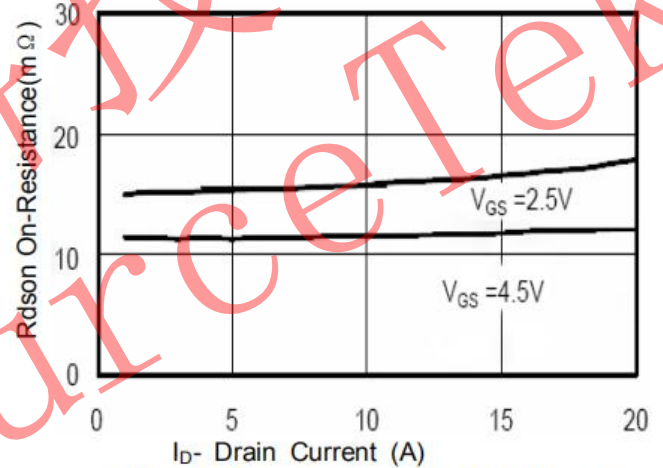


Figure 4 Drain-Source On-Resistance

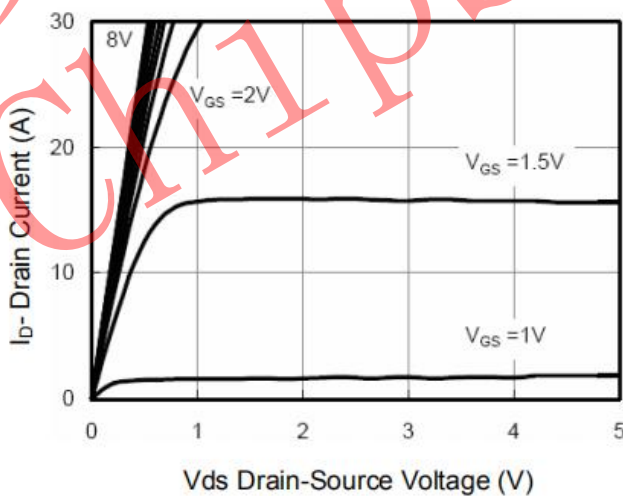


Figure 5 Output CHARACTERISTICS

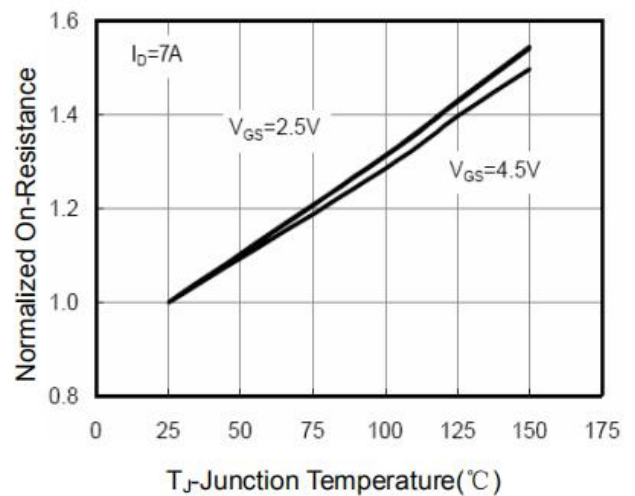


Figure 6 Drain-Source On-Resistance

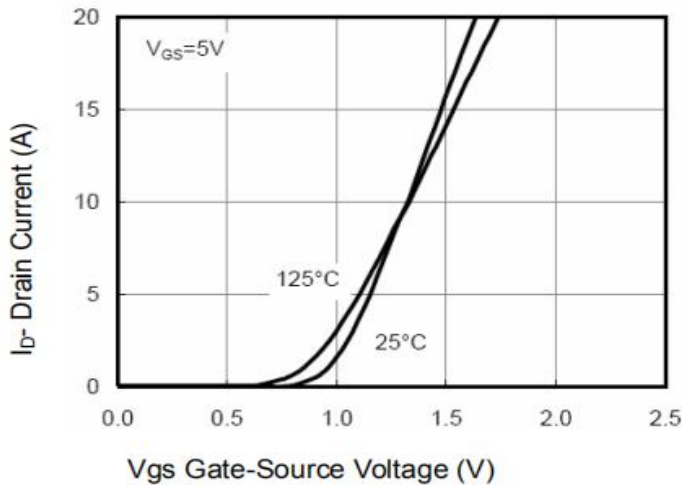


Figure 7 Transfer Characteristics

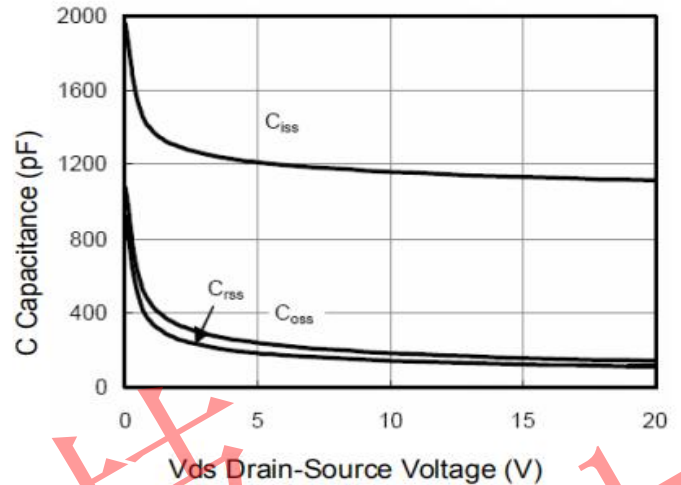


Figure 8 Capacitance vs Vds

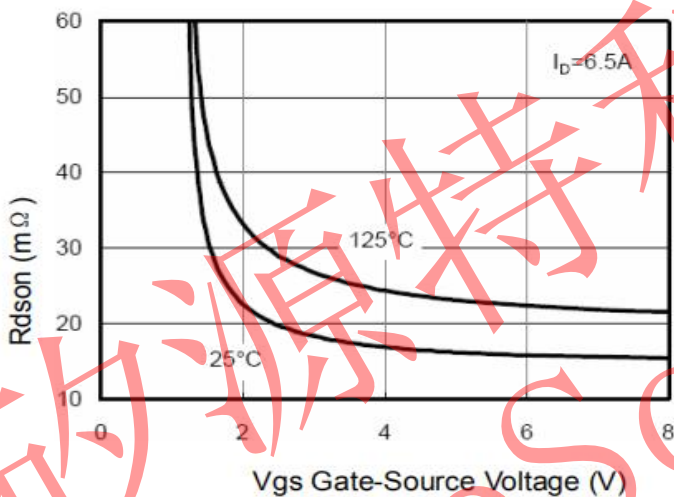


Figure 9 Rdson vs Vgs

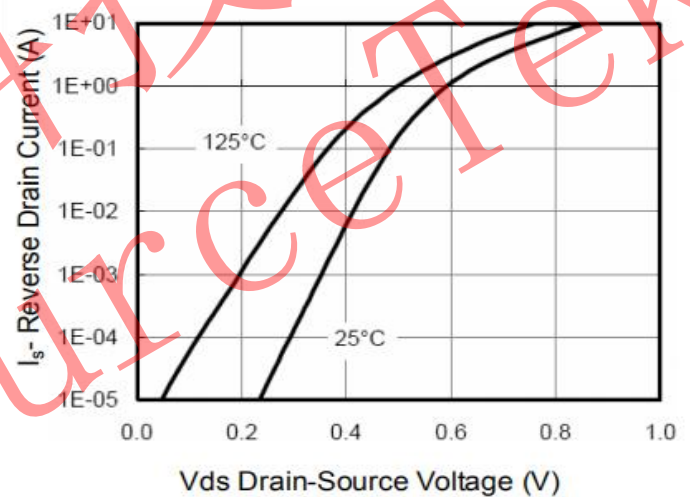


Figure 10 Capacitance vs Vds

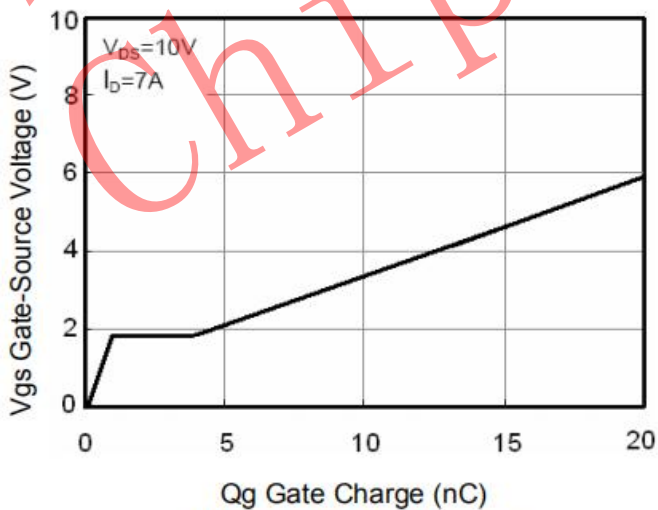


Figure 11 Gate Charge

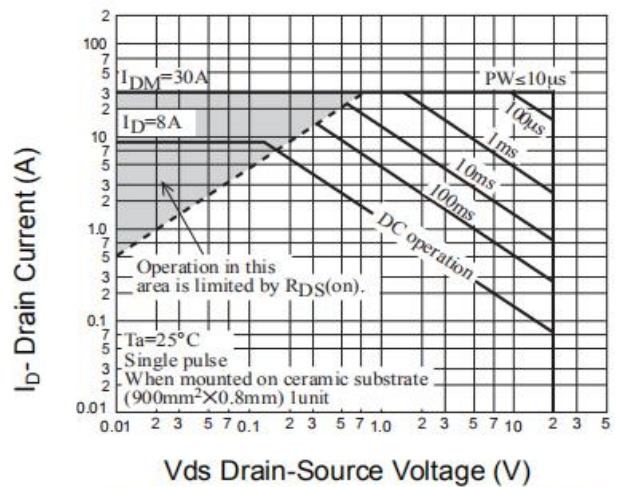
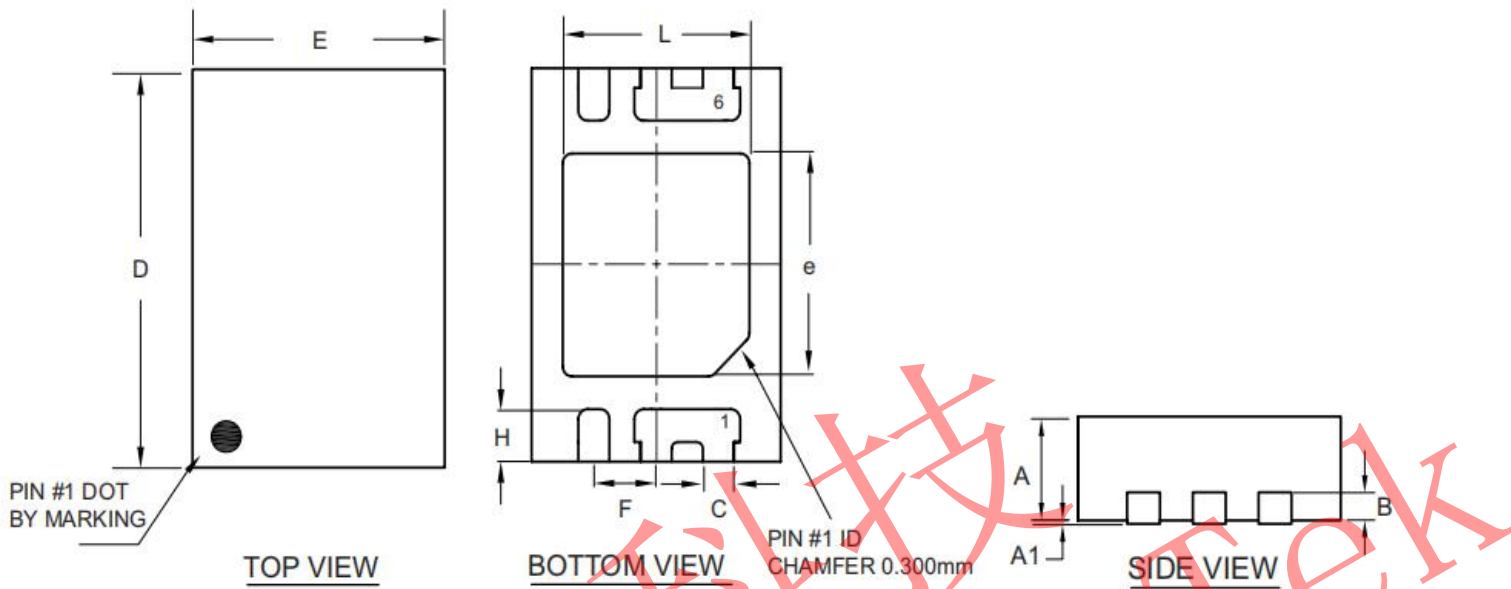


Figure 12 Safe Operation Area



DFN2x3-6L PACKAGE OUTLINE DIMENSIONS



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
D	2.950	3.050	0.116	0.120
E	1.950	2.050	0.077	0.081
H	0.350	0.450	0.014	0.018
L	1.450	1.550	0.057	0.061
e	1.650	1.750	0.065	0.069
B	0.195	0.211	0.0076	0.008
C	0.200	0.300	0.008	0.012
F	0.500 BSC		0.020 BSC	

