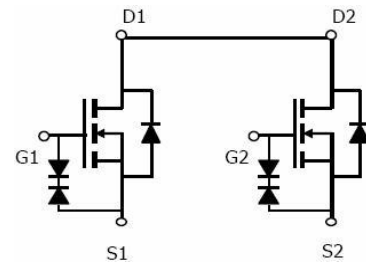




## Dual N-Channel Enhancement Mode Power MOSFET

### Description

The MX3382 uses advanced trench technology to provide excellent  $R_{DS(ON)}$ , low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected

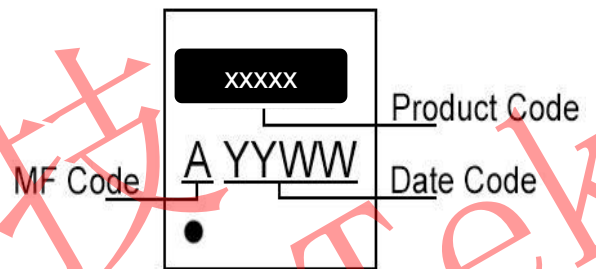


Schematic diagram

### General Features

- ◆  $V_{DS} = 18V$ ,  $I_D = 22A$
  - ◆ @ $V_{GS} = 4.5V$   $R_{DS(ON)}$ (Typ.) = 4.5m $\Omega$
  - ◆ @ $V_{GS} = 3.8V$   $R_{DS(ON)}$ (Typ.) = 4.7m $\Omega$
  - ◆ @ $V_{GS} = 2.5V$   $R_{DS(ON)}$ (Typ.) = 6m $\Omega$
- ESD Rating: 2000V HBM

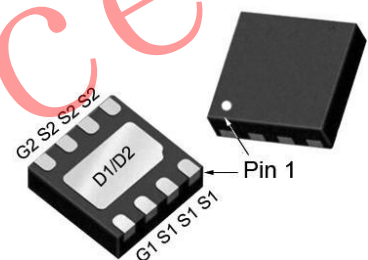
High Power and current handing capability  
Lead free product is acquired  
Surface Mount Package



Marking and pin Assignment

### Application

PWM application  
Load switch



DFN3x3-8L top view

### Absolute Maximum Ratings (TA=25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	18	V
Gate-Source Voltage		$V_{GS}$	$\pm 12$	
Continuous Drain Current	$T_A = 25^\circ C$	$I_D$	22	A
	$T_A = 70^\circ C$		16	
Pulsed Drain Current (Note 1)		$I_{DM}$	80	A
Avalanche Current		$I_{AS}$	20	
Avalanche Energy	$L = 0.1mH$	$E_{AS}$	26	mJ
Power Dissipation	$T_A = 25^\circ C$	$P_D$	3.6	W
	$T_A = 70^\circ C$		2.4	
Operating Junction & Storage Temperature Range		$T_J, T_{stg}$	-55 to 150	$^\circ C$



### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	34.7	$^{\circ}C/W$
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### Notes:

1. Pulse width limited by maximum junction temperature.
2. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^{\circ}C$ .

### Electrical Characteristics ( $T_A = 25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	18	20	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$	-	-	1	$\mu A$
<b>Parameter</b>						
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$	-	-	$\pm 10$	$\mu A$
<b>On Characteristics (Note 2)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.8	1.2	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=8A$	2.9	3.4	4.5	m $\Omega$
		$V_{GS}=3.8V, I_D=7A$	3	3.5	4.7	m $\Omega$
		$V_{GS}=2.5V, I_D=6A$	3.8	4.4	6	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=5A$	-	40	-	S
<b>Dynamic Characteristics (Note 3)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V,$ $F=1.0MHz$	-	3140	-	PF
Output Capacitance	$C_{oss}$		-	352	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	320	-	PF
<b>Switching Characteristics (Note 3)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10V, R_L=1.35\Omega$ $V_{GS}=5V, R_{GEN}=3\Omega$	-	20	-	nS
Turn-on Rise Time	$t_r$		-	40	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	72	-	nS
Turn-Off Fall Time	$t_f$		-	16	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=10V, I_D=7A,$ $V_{GS}=4.5V$	-	35	-	nC
Gate-Source Charge	$Q_{gs}$		-	3	-	nC
Gate-Drain Charge	$Q_{gd}$		-	10	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 2)	$V_{SD}$	$V_{GS}=0V, I_S=1A$	-	-	1.2	V
Diode Forward Current (Note 1)	$I_S$		-	-	26	A

### Notes:

1. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
2. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
3. Guaranteed by design, not subject to production



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

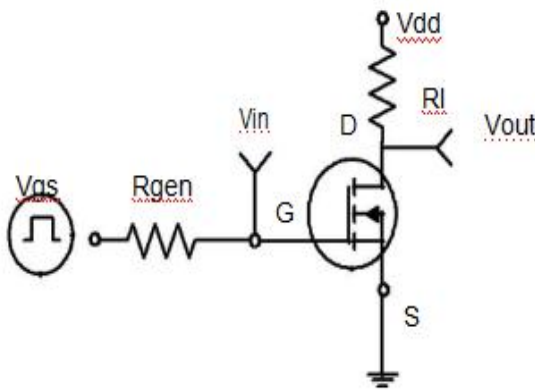


Figure 1: Switching Test Circuit

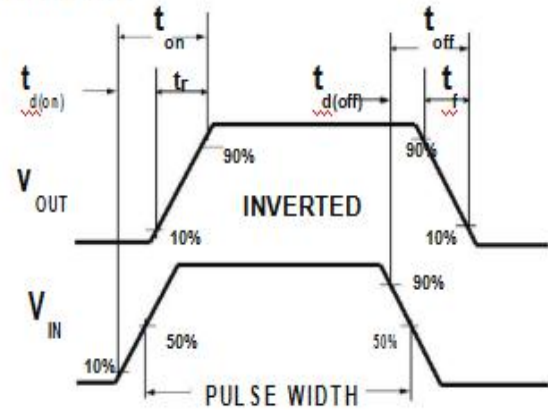
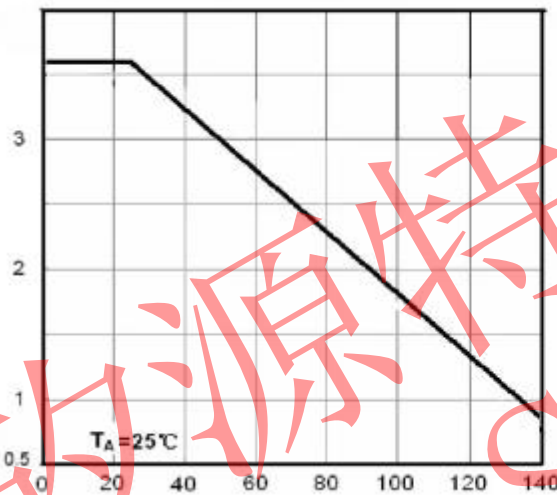
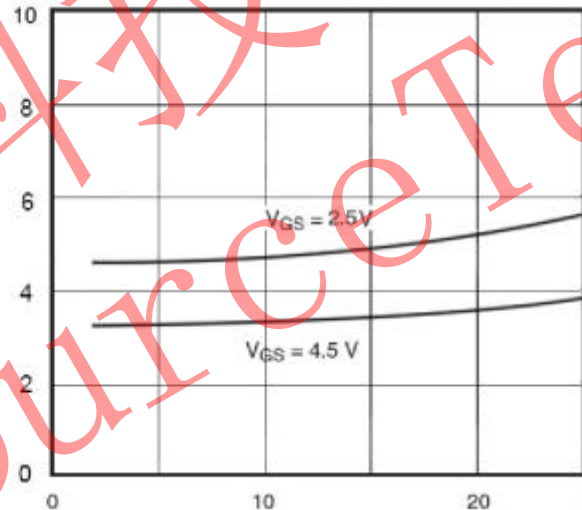


Figure 2: Switching Waveforms



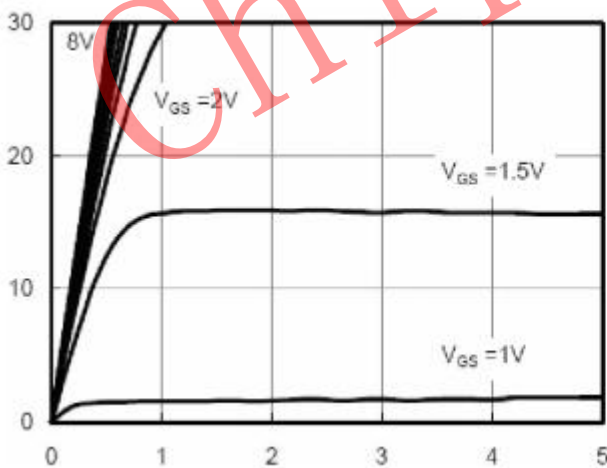
T<sub>J</sub>-Junction Temperature(°C)

Figure 3 Power Dissipation



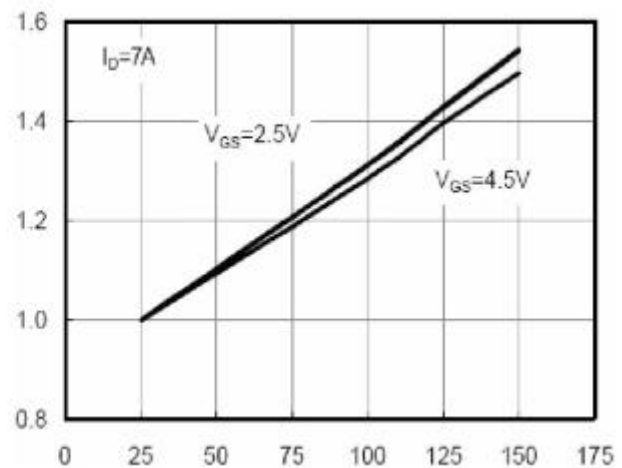
ID- Drain Current (A)

Figure 4 Drain-Source On-Resistance



Vds Drain-Source Voltage (V)

Figure 5 Output CHARACTERISTICS



T<sub>J</sub>-Junction Temperature(°C)

Figure 6 Drain-Source On-Resistance

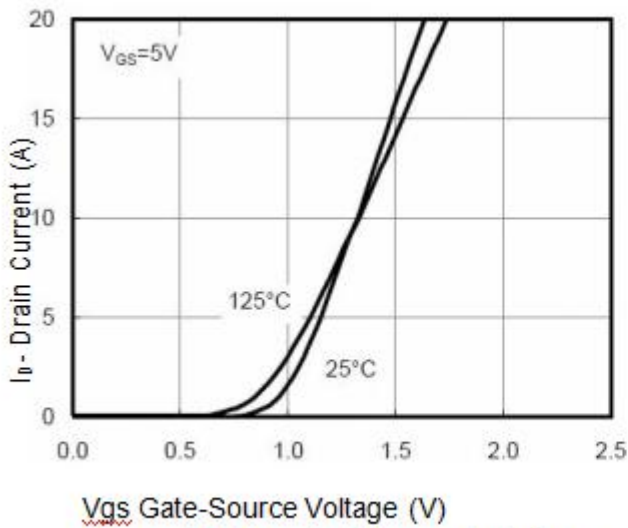


Figure 7 Transfer Characteristics

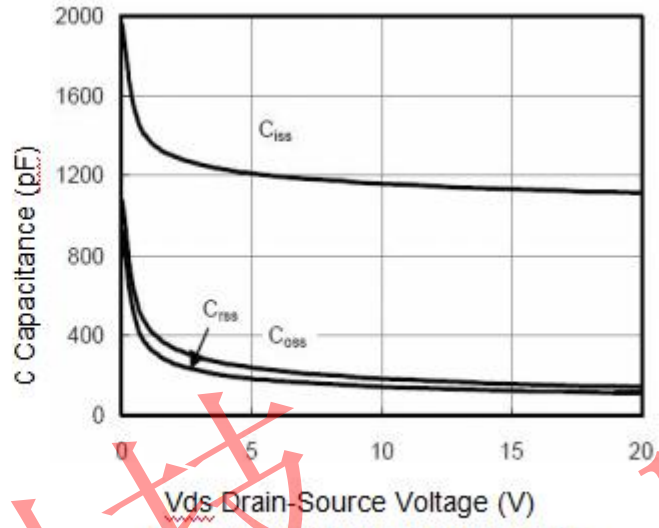


Figure 8 Capacitance vs Vds

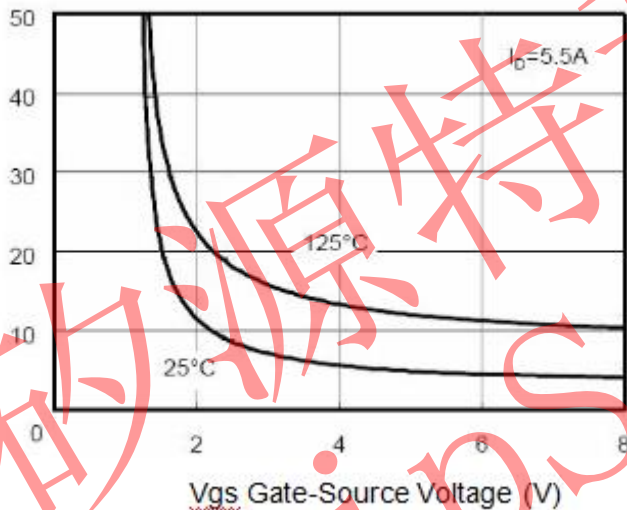


Figure 9 Rds(on) vs Vgs

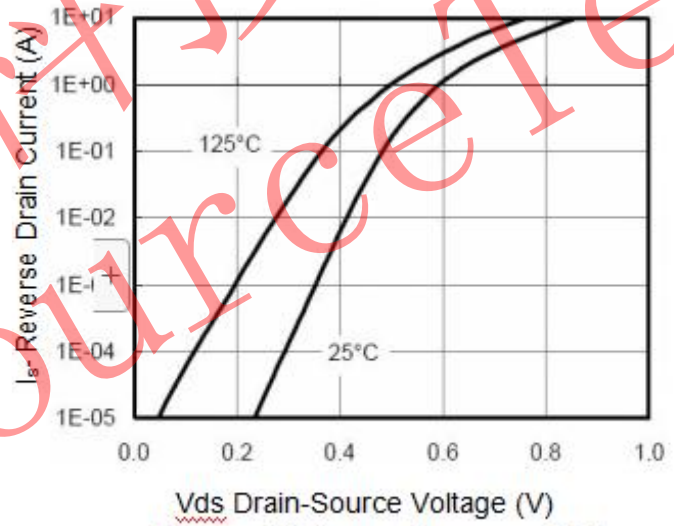


Figure 10 Capacitance vs Vds

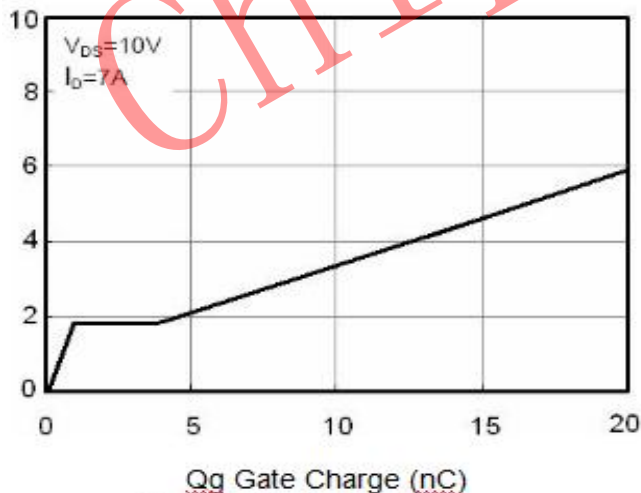


Figure 11 Gate Charge

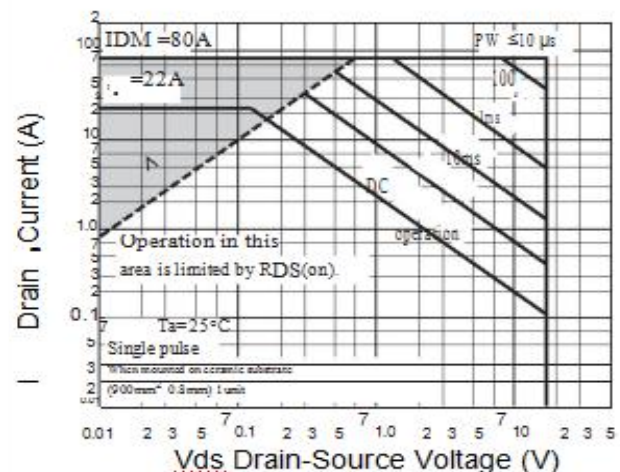
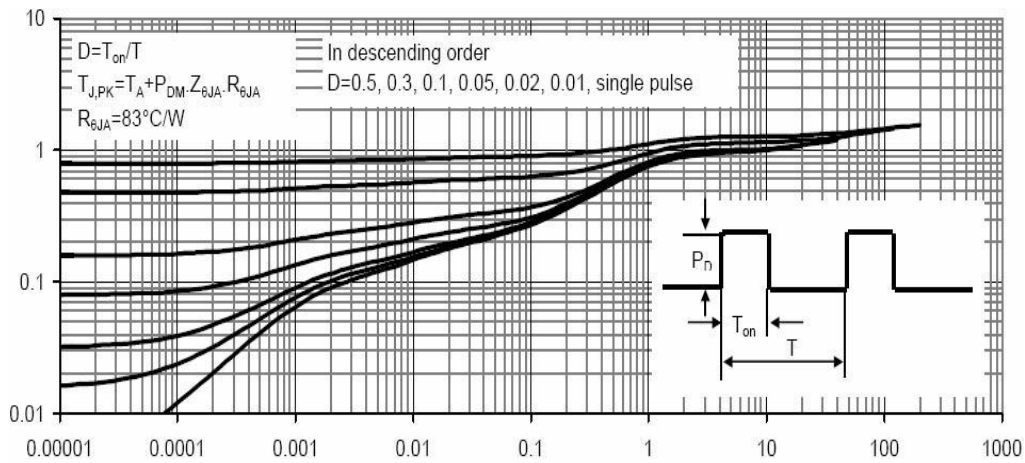


Figure 12 Safe Operation Area



Square Wave Pluse Duration(sec)

Figure 13 Normalized Maximum Transient Thermal Impedance



Package Dimension

DFN 3x3 MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	0.7		0.8	I		0.203	
B	0.25		0.35	J	2.2		2.4
C	0.2			K	1.4		1.6
D	2.924		3.076				
E	2.924		3.076				
F	0.324		0.476				
G		0.65					
H	0		0.05				

