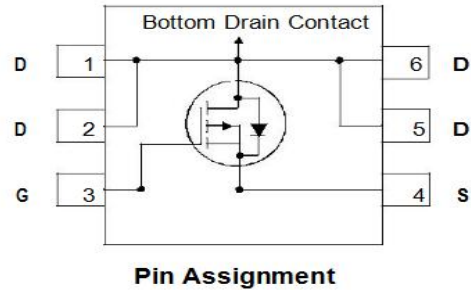




P-Channel Enhancement Mode Power MOSFET

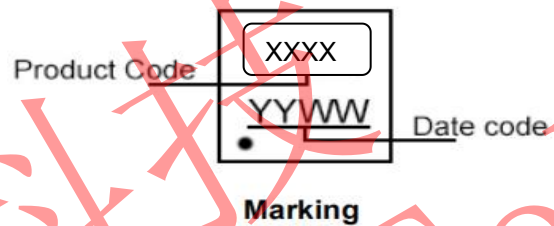
Description

The MXND805 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switching applications and a wide variety of other applications.



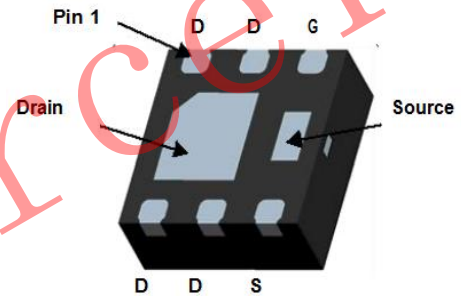
General Features

- ◆ $V_{DS} = -12V$, $I_D = -8.5A$
 @ $V_{GS} = -4.5V$ $R_{DS(ON)}(Typ.) = 14m\Omega$
 @ $V_{GS} = -2.5V$ $R_{DS(ON)}(Typ.) = 19m\Omega$
 @ $V_{GS} = -1.8V$ $R_{DS(ON)}(Typ.) = 29m\Omega$
- ◆ Advanced trench MOSFET process technology
- ◆ Ultra low on-resistance with low gate charge
- ◆ New Thermally Enhanced DFN2X2-6L Package



Application

- ◆ PWM applications
- ◆ Load switch
- ◆ battery charge in cellular handset



DFN2x2-6L Pin definition and Top / Bottom View

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-12	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous	I_D	-8.5	A
Drain Current-Pulsed (Note 1)	I_{DM}	-32	A
Maximum Power Dissipation	P_D	2.8	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C



Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-12	-15	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-12V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±12V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-0.4	-0.65	-1.0	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} =-4.5V, I _D =-6A	-	14	18	mΩ
		V _{GS} =-2.5V, I _D =-5A	-	19	25	
		V _{GS} =-1.8V, I _D =-2.5A	-	29	45	
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-8A	-	33	-	S
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-1A	-	-	-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-3.5	A
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-6V, V _{GS} =0V, F=1.0MHz	-	1370	-	PF
Output Capacitance	C _{oss}		-	350	-	PF
Reverse Transfer Capacitance	C _{rss}		-	258	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-6V, R _L =0.75Ω V _{GS} =-4.5V, R _{GEN} =3Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	25	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	42	-	nS
Total Gate Charge	Q _g		-	13	-	nC
Gate-Source Charge	Q _{gs}		V _{DS} =-6V, I _D =-8A, V _{GS} =-4.5V	-	2	-
Gate-Drain Charge	Q _{gd}		-	3	-	nC

Notes:

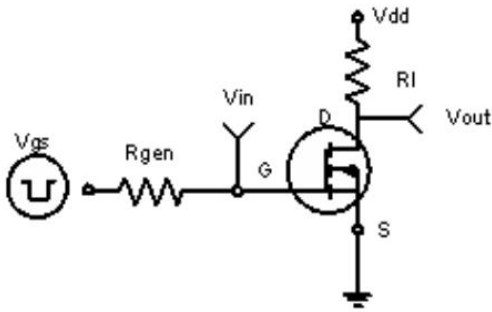
- surface mounted on FR4 board, t≤10sec
- pulse test: pulse width≤300μs, duty≤2%
- guaranteed by design, not subject to production testing

Thermal Characteristics

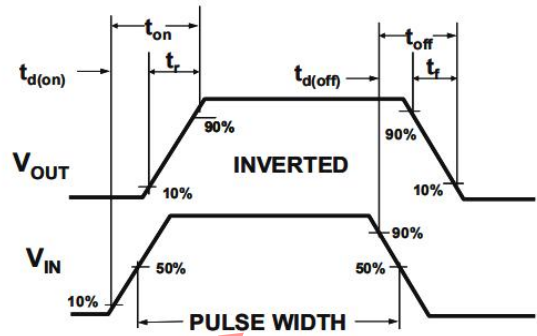
Thermal Resistance junction-to ambient	R _{th JA}	45	°C/W
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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



Switching Test Circuit



Switching Waveforms

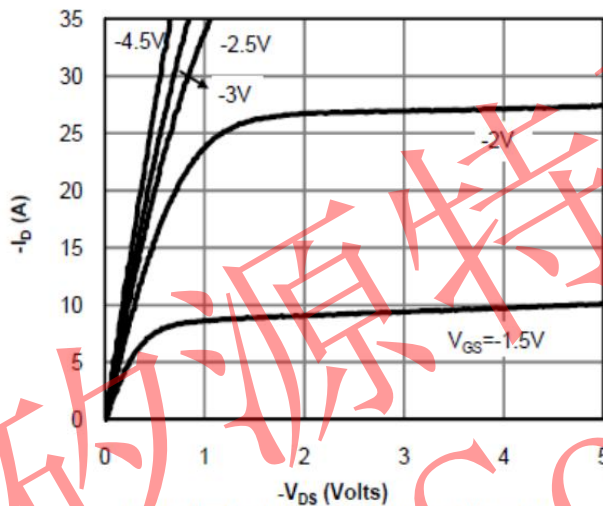


Fig 1: On-Region Characteristics (Note E)

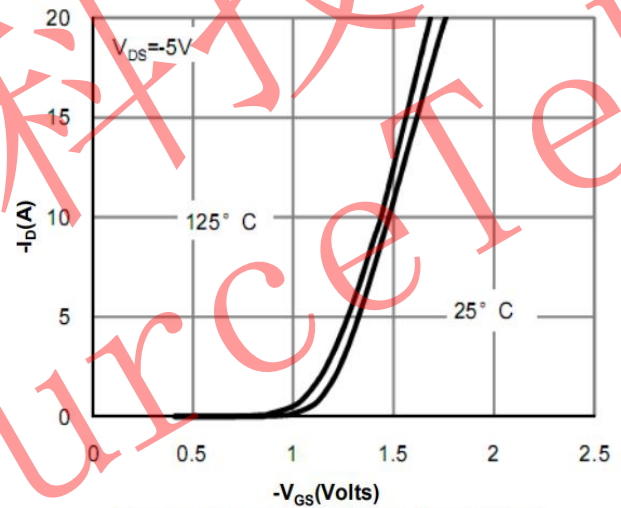


Figure 2: Transfer Characteristics (Note E)

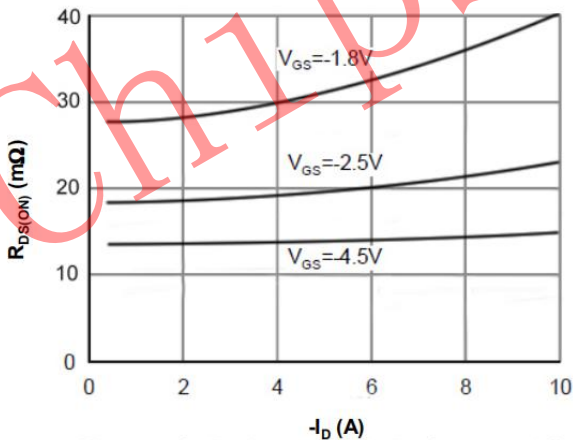


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

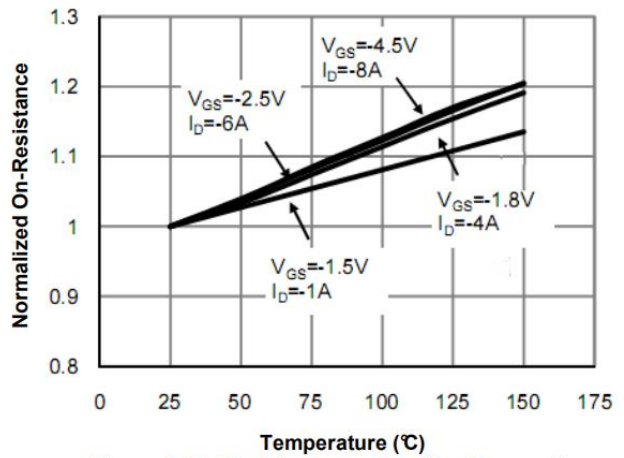


Figure 4: On-Resistance vs. Junction Temperature (Note E)

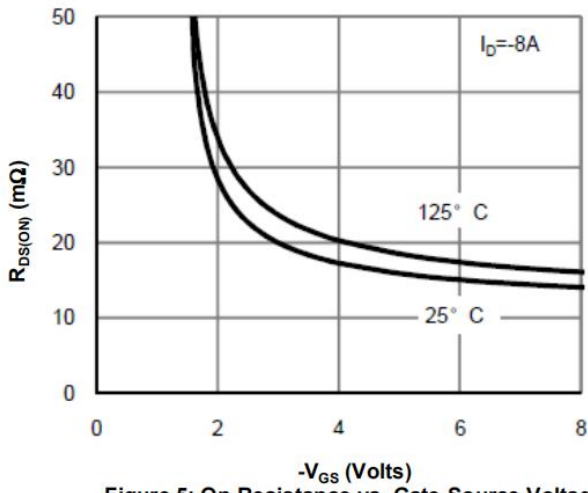


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

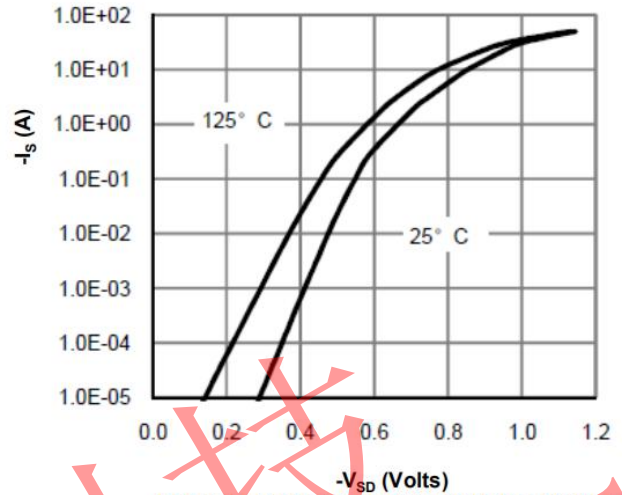


Figure 6: Body-Diode Characteristics (Note E)

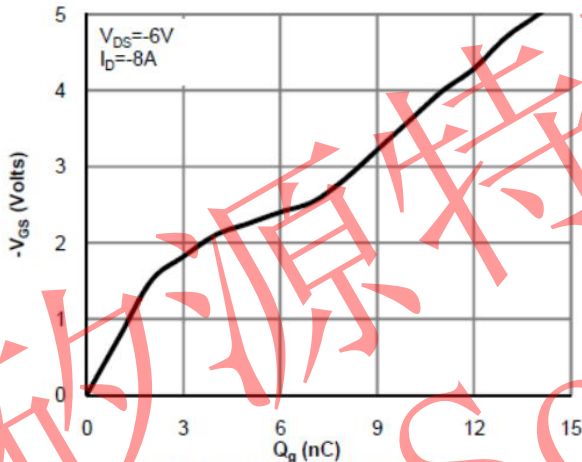


Figure 7: Gate-Charge Characteristics

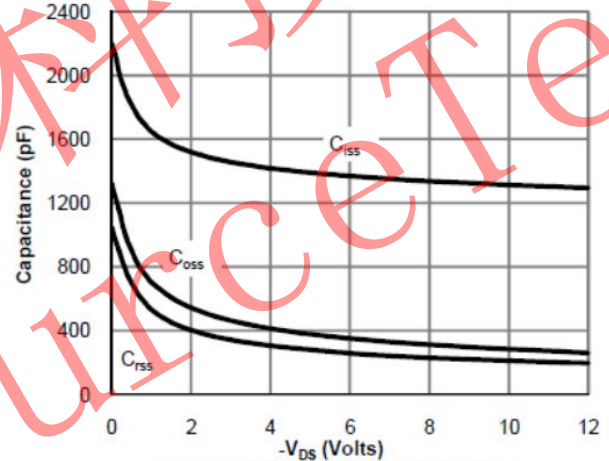


Figure 8: Capacitance Characteristics

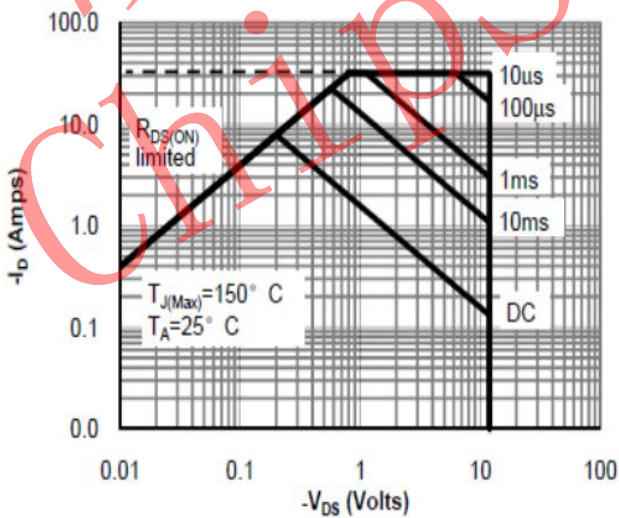


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

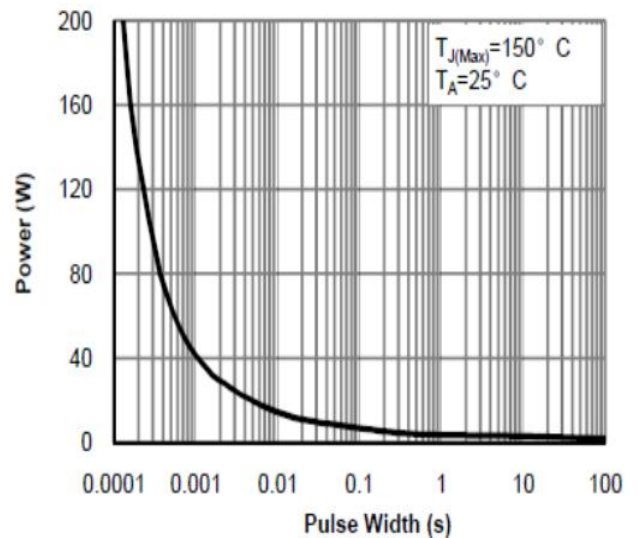


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note H)

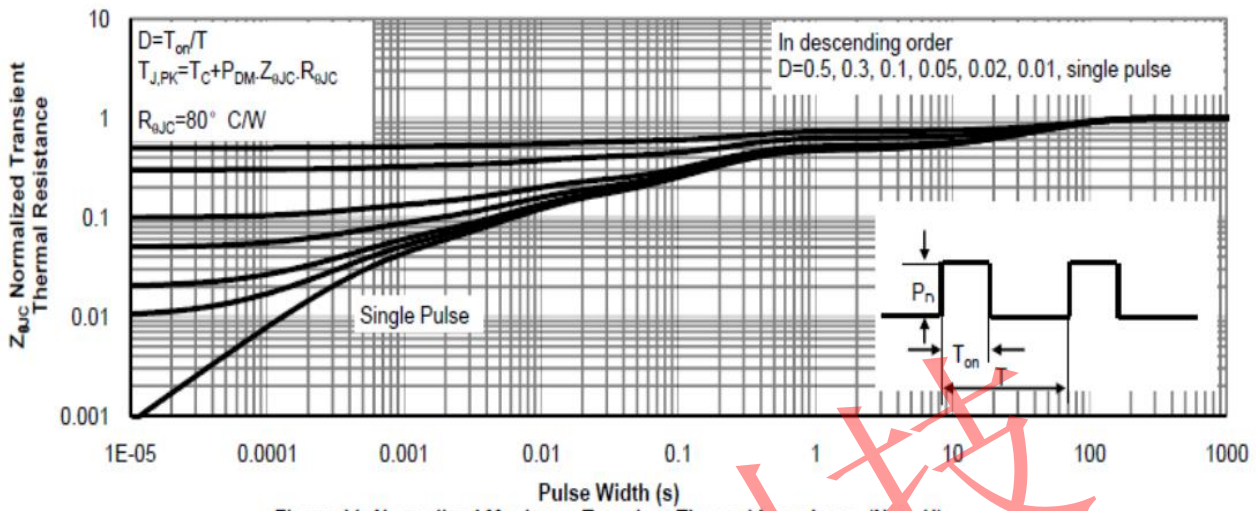
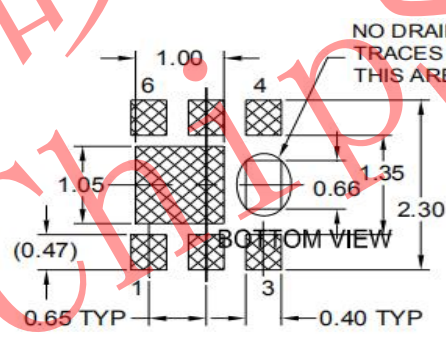
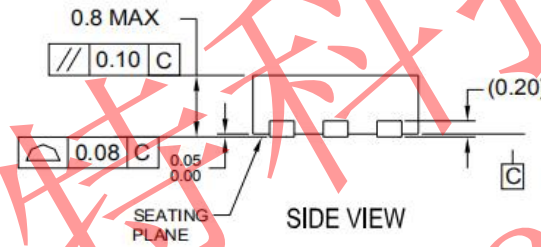
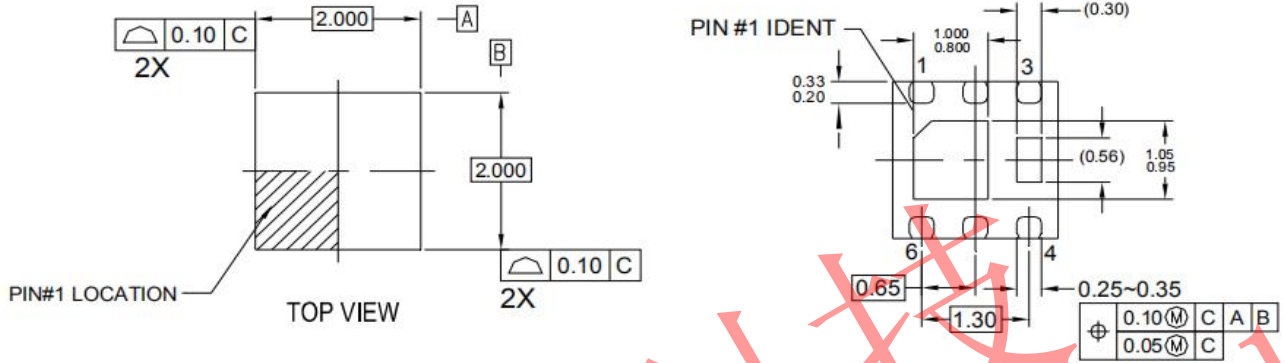


Figure 11: Normalized Maximum Transient Thermal Impedance (Note H)

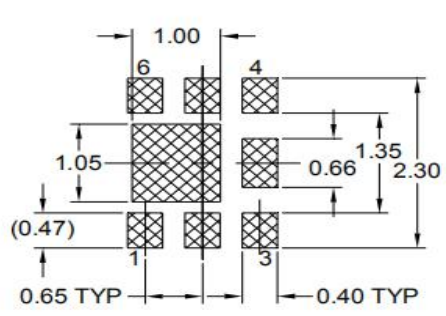
矽源特科技
ChipSourceTek



DFN2x2-6L PACKAGE OUTLINE DIMENSIONS



RECOMMENDED LAND PATTERN OPT 1



RECOMMENDED LAND PATTERN OPT 2

NOTES

1. All dimensions are in millimeters.
2. Tolerance $\pm 0.10\text{mm}$ (4 mil) unless otherwise specified
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.