PAM8908

25-mW TrueCapFree Stereo Headphone Amplifier

Key Features

- Patent Pending 3 Phase Power Line Shift Charge Pump Eliminates Need for DC-Blocking Capacitors
- TrueCapFree Architecture, Output Biased at 0V (System Ground)
- Excellent Low Frequency Fidelity
- High PSRR
- Less Than 1uA Shutdown Current
- Support Both Fully Differential and Single-Ended Inputs
- Short Circuit and Over Temperature Protection
- Selectable Gain Settings:-6dB,0dB,3dB and 6dB
- Available in Space Saving Packages: TQFN3x3-16L

Applications

- Smart Phones/Cellular Phones
- Notebook Computers
- Portable DVD Player
- Personal Digital Assistants (PDAs)
- Electronic Dictionaries
- Digital Still Cameras
- Potable Gaming

General Description

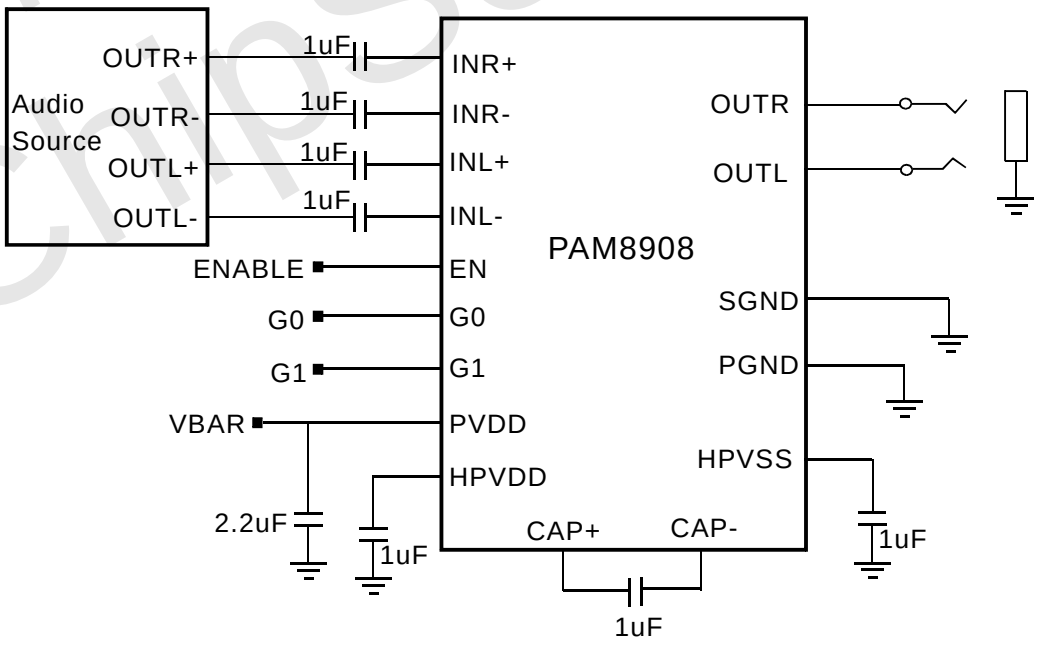
The PAM8908 stereo headphone driver is designed for portable equipment where board space is at a premium. The PAM8908 uses a unique, patent pending architecture to produce a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, board space, and component height.

The PAM8908 delivers up to 25mW per channel into a 16Ω load and has low 0.03% THD+N. A high power-supply rejection ratio allows this device to operate from noisy digital supplies without an additional linear regulator.

The PAM8908 operates from a single supply from 2.5V to 5.5V, has short-circuit and over temperature protection. Shutdown mode reduces supply current to less than 1uA.

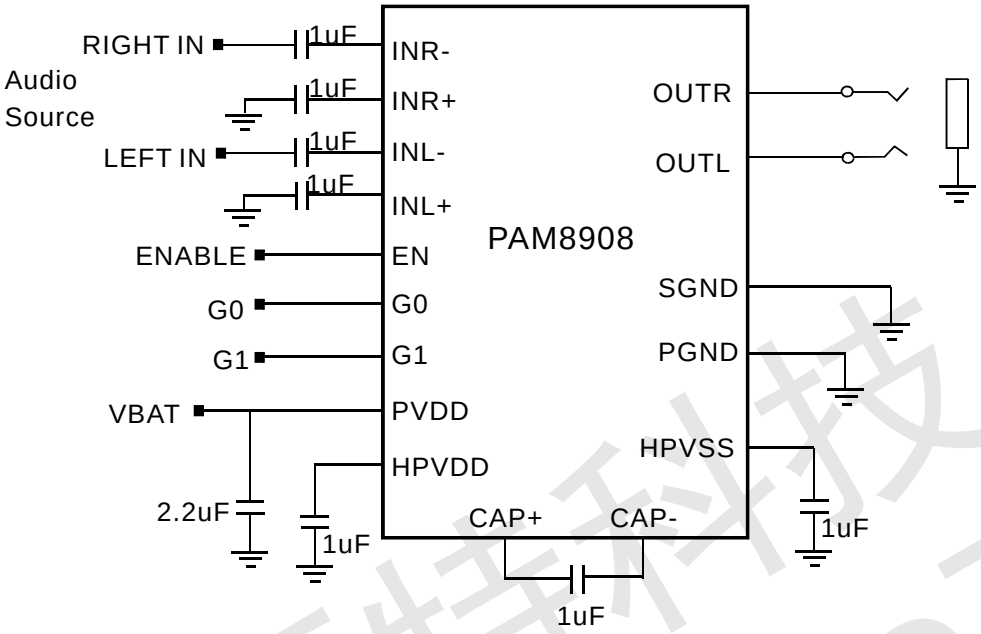
Typical Application Circuit

Typical Application Configuration with Differential Input Signals

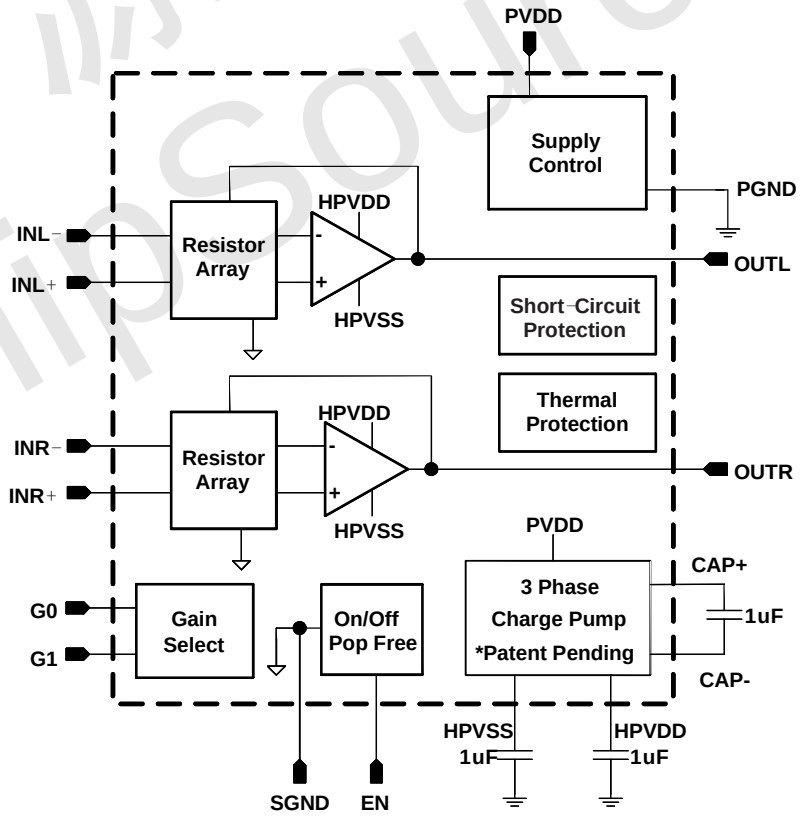


Typical Application Circuit

Typical Application Configuration with Single-Ended Input Signal

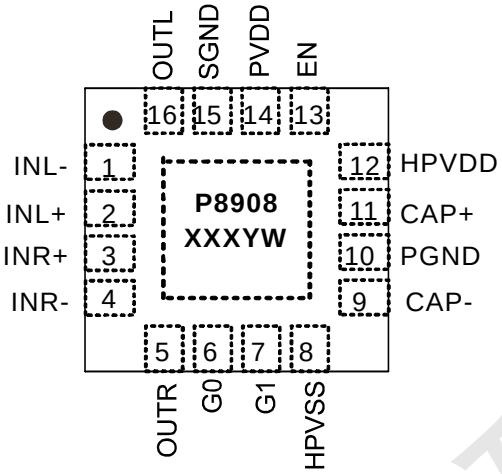


Block Diagram



Pin Configuration & Marking Information

Top View
TQFN3X3-16L



X: Internal Code
Y: Year
W: Week

Pin Description

PIN NO.	PIN NAME	I/O/P	DESCRIPTION
1	INL-	I	Inverting left input for differential signals
2	INL+	I	Non-inverting left input for differential signals.
3	INR+	I	Inverting right input for differential signals
4	INR-	I	Non-inverting right input for differential signals
5	OUTR	O	Right headphone amplifier output. Connect to right terminal of headphone jack.
6	G0	I	Gain select bit 0
7	G1	I	Gain select bit 1
8	HPVSS	P	Charge pump output and negative power supply for output amplifiers; connect 1uF capacitor to GND
9	CAP-	O	Charge pump negative flying cap.
10	PGND	P	Power Ground
11	CAP+	O	Charge pump positive flying cap.
12	HPVDD	O	Positive power supply for headphone amplifiers. Charge pump positive half vdd output.
13	EN	I	Amplifier enable. Connect to logic low to shutdown; connect to logic high to activate
14	PVDD	P	Power Vdd.
15	SGND	I	Amplifier reference voltage.
16	OUTL	O	Left headphone amplifier output. Connect to left terminal of headphone jack.

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage(PVDD).....6.0V
Input Voltage(INR+, INR-, INL+, INL-).....
.....HPVSS-0.3V to HPVDD+0.3V
Control Interface Voltage(G0, G1, EN).....
.....-0.3V to PVDD+0.3V

Storage Temperature.....-65°C to 150°C
Maximum Junction Temperature.....150°C
Soldering Temperature.....250°C,10 sec

Recommended Operating Conditions

Supply Voltage Range.....2.5V to 5.5V

Ambient Temperature Range.....-40°C to 85°C
Junction Temperature Range.....-40°C to 125°C

Thermal Information

Parameter	Symbol	Package	Maximum	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	TQFN 3x3-16	35	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	TQFN 3x3-16	14	°C/W

Electrical Characteristic

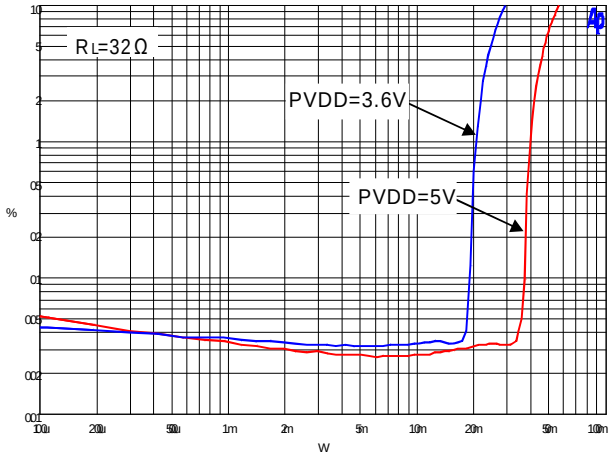
T_A=25°C,PVDD=3.6V, RL=16Ω (unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	PVDD		2.5		5.5	V
Quiescent Current	I_Q	EN=PVDD, No load		4		mA
Output Power per Channel	P_O	THD=1%, f=1kHz, RL=16Ω		35		mW
		THD=1%, f=1kHz, RL=32Ω		25		
Shutdown Current	Isd	EN=0V, PVDD=2.5V to 5.5V		0.1	1	uA
EN High level input voltage	VIH		1.4			V
EN Low level input voltage	VIL				0.6	V
G0,G1 High level input voltage	VGH		1.4			V
G0,G1 Low level input voltage	VGL				0.6	V
Output Offset voltage	Vos			1	3	mV
Closed-loop voltage gain	AV	G0=0V, G1=0V		-6		dB
		G0=PVDD,G1=0V		0		dB
		G0=0V,G1=PVDD		3		dB
		G0=PVDD,G1=PVDD		6		dB
Power supply rejection ratio	PSRR	Input AC-GND, f=1KHz, Vpp=200mV		75		dB
Total Harmonic distortion plus noise	THD+N	Po=20mW,f=1kHz		0.03		%
Signal to noise ratio	SNR	Po=20mW into 16Ω		100		dB
Noise output voltage	En	A-weighted		10		uVrms
Corsstalk	CS	Po=15mW,f=1kHz		80		dB
Chargepump switching frequency	Fosc		1.2	1.5	1.8	MHz
start-up time	Ton	EN from low to high		0.4		mS
Thermal shutdown	OTP	Threshold		150		°C
Thermal shutdown Hysteresis	OTPH	Hysteresis		20		°C

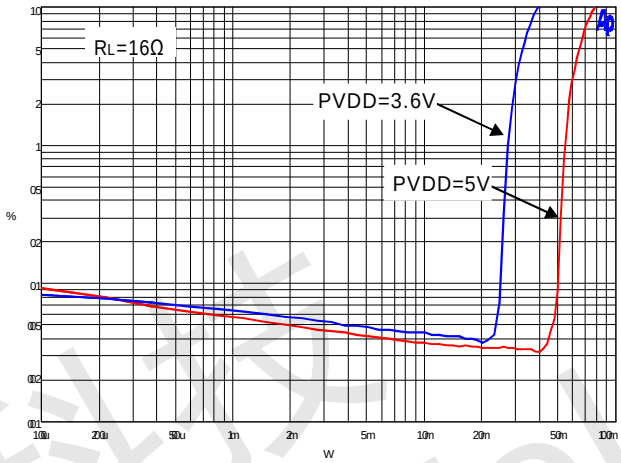
Typical Operating Characteristics

T_A=25°C, PVDD=3.6V, f=1kHz, Gain=6dB, unless otherwise.

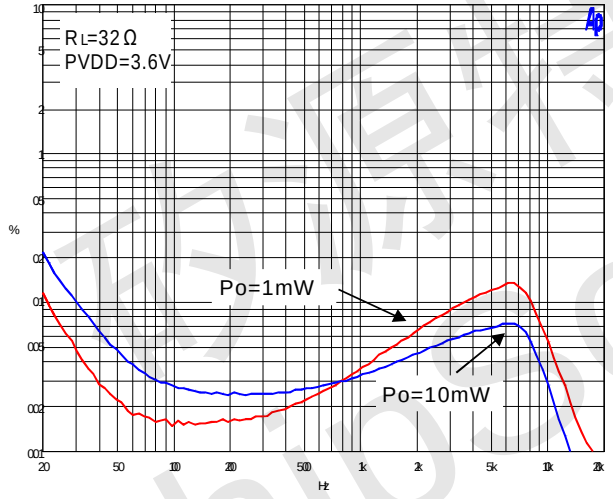
1. THD+N vs Output Power



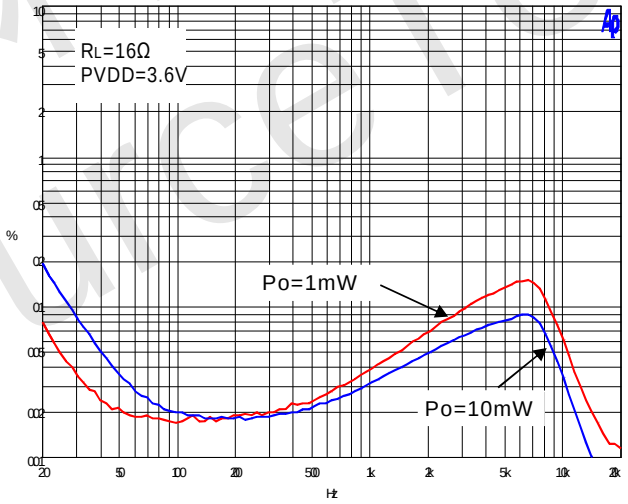
2. THD+N vs Output Power



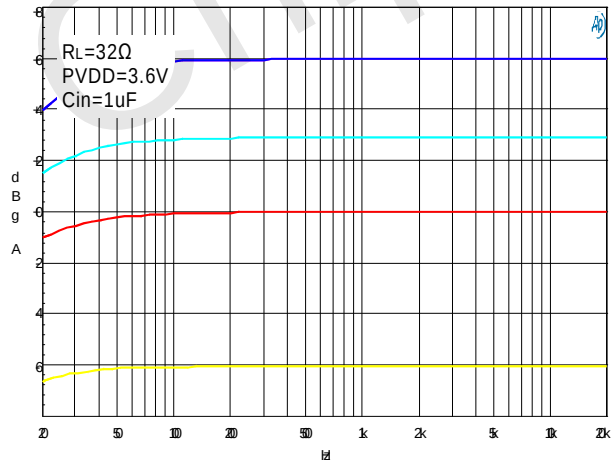
3. THD+N vs Frequency



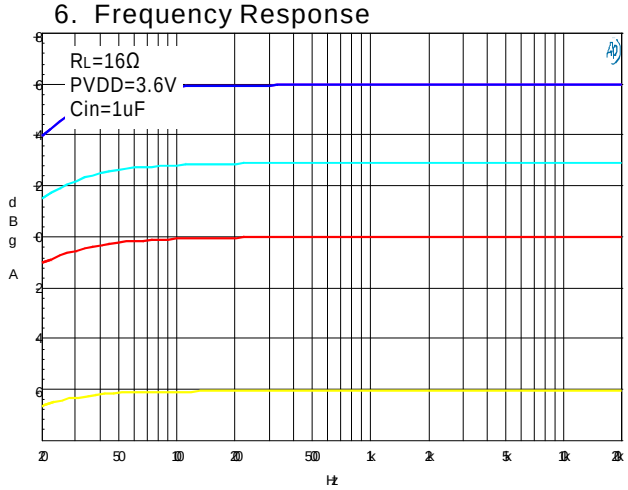
4. THD+N vs Frequency



5. Frequency Response



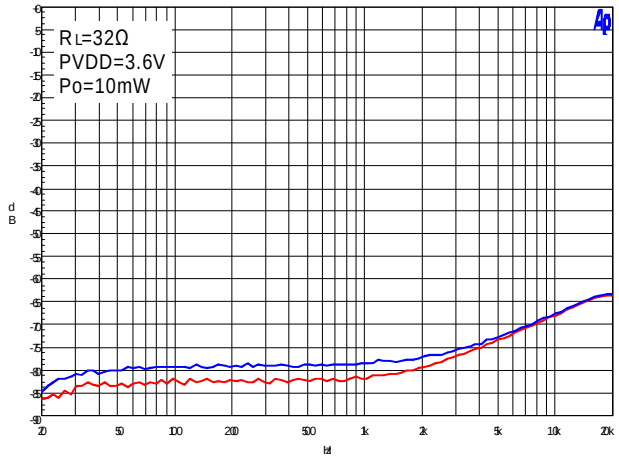
6. Frequency Response



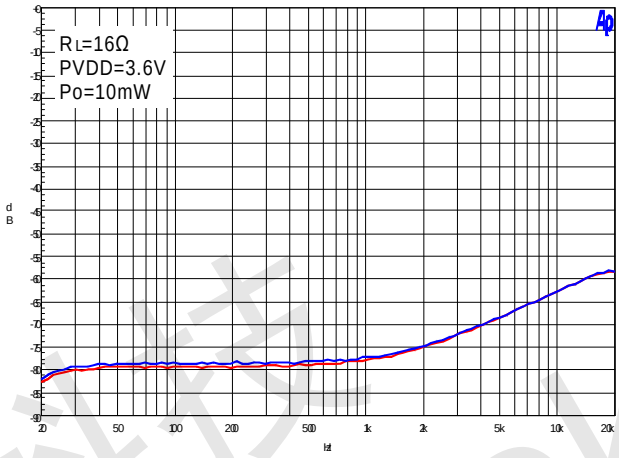
Typical Operating Characteristics

T_A=25°C, PVDD=3.6V, f=1kHz, Gain=6dB, unless otherwise.

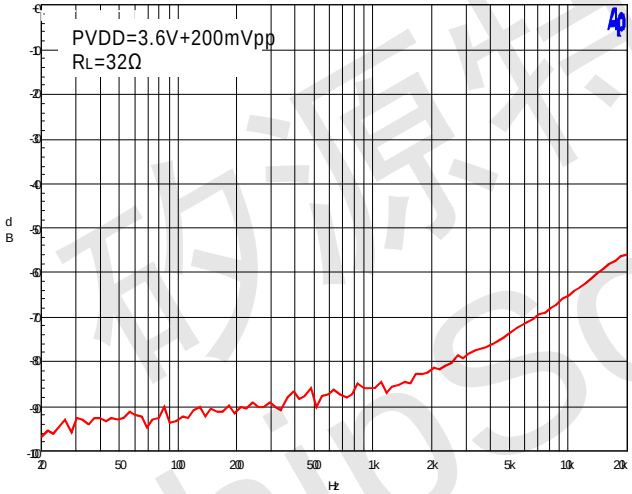
7. Crosstalk



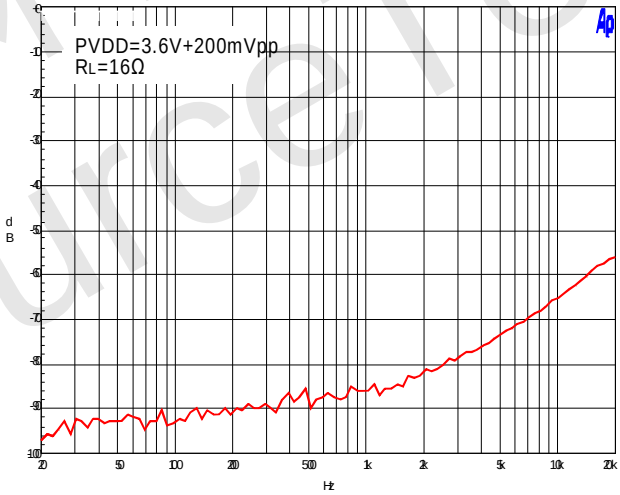
8. Crosstalk



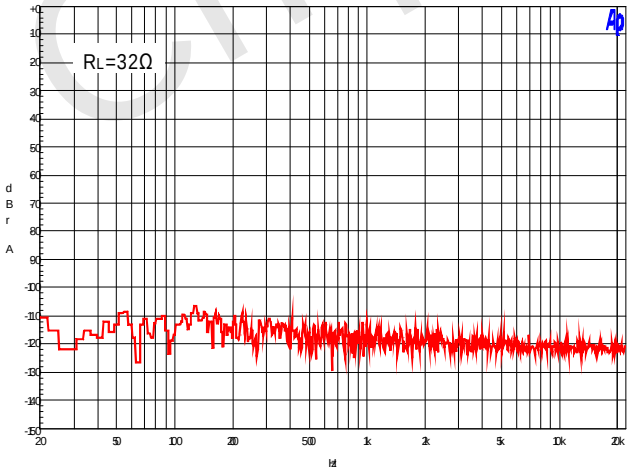
9. PSRR



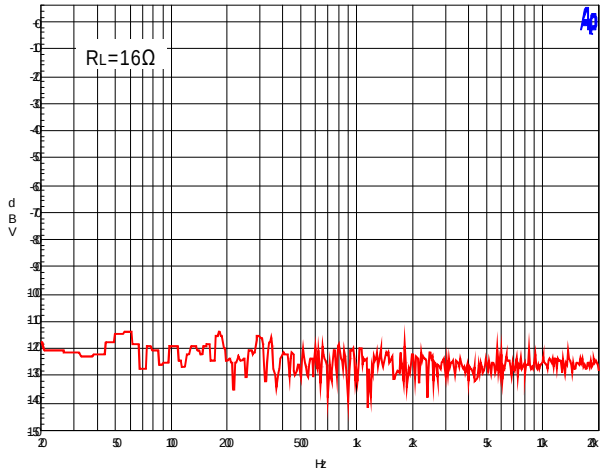
10. PSRR



11. FFT Noise



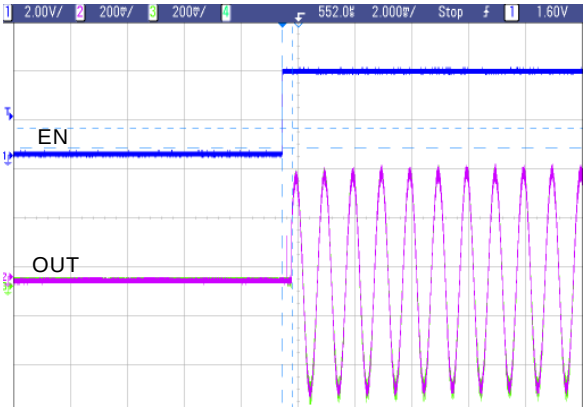
12. FFT Noise



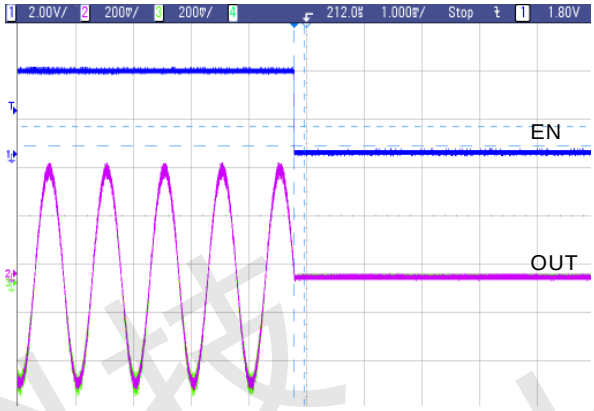
Typical Operating Characteristics

T_A=25°C, PVDD=3.6V, f=1kHz, Gain=6dB, unless otherwise.

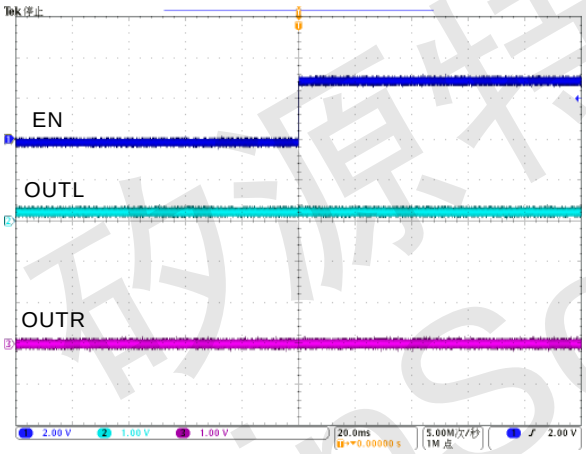
13. Start up with signal



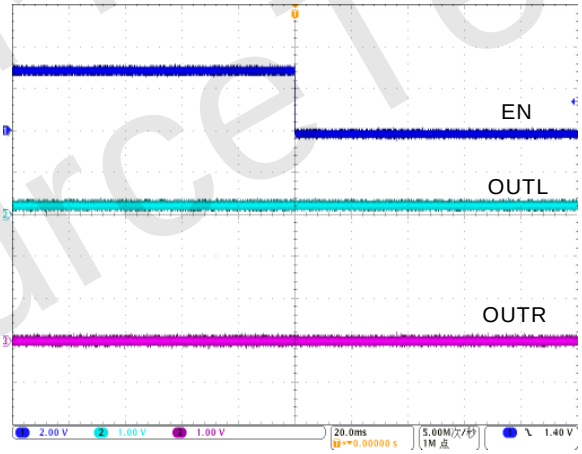
14. Shutdown with signal



15. Start up without signal



16. Shutdown without signal



Application Information

The basic PAM8908 application circuit is shown in page 1 and page 2.

GAIN CONTROL

The PAM8908 has four gain settings which are controlled with pins G0 and G1. The following table gives an overview of the gain function.

G0 VOLTAGE	G1 VOLTAGE	AMPLIFIER GAIN
≤0.6 V	≤0.6 V	–6 dB
≥1.4 V	≤0.6 V	0 dB
≤0.6 V	≥1.4 V	3 dB
≥1.4 V	≥1.4 V	6 dB

INPUT COUPLING CAPACITORS

Input coupling capacitors block any DC bias from the audio source and ensure maximum dynamic range. Input coupling capacitors also minimize PAM8908 turn-on pop to an inaudible level.
The input capacitors are in series with PAM8908 internal input resistors, creating a high-pass filter. The following Equation calculates the high-pass filter corner frequency.

$$f_C = \frac{1}{2\pi R_{IN} C_{IN}}$$

The input impedance, RIN, is dependent on device gain. Larger input capacitors decrease the corner frequency. See the following table for input impedance values.

G0 VOLTAGE	G1 VOLTAGE	RIN
≤0.6 V	≤0.6 V	26.4kΩ
≥1.4 V	≤0.6 V	19.8kΩ
≤0.6 V	≥1.4 V	16.5kΩ
≥1.4 V	≥1.4 V	13.2kΩ

For a given high-pass cutoff frequency, the minimum input coupling capacitor is found as:

$$C_{IN} = \frac{1}{2\pi f_C R_{IN}}$$

Example: Design for a 20Hz corner frequency with a PAM8908 gain of +6dB. The input impedance table gives RIN as 13.2kΩ. The CIN Equation shows the input coupling capacitors must be at least 0.6uF to achieve a 20Hz high-pass corner frequency. Choose a 0.68uF standard value capacitor for each PAM8908 input (X5R material or better is required for best performance).

CHARGE PUMP FLYING CAPACITOR, HPVDD CAPACITOR AND HPVSS CAPACITOR

The PAM8908 uses a built-in charge pump to generate a positive and negative voltage supply for the headphone amplifiers. The charge pump flying capacitor connects between CAP+ and CAP-. It transfers charge to generate the positive and negative supply voltage. The HPVDD capacitor or HPVSS capacitor must be at least equal in or larger than value to the flying capacitor to allow maximum charge transfer. Use low equivalent-series-resistance (ESR) ceramic capacitors (X5R material or better is required for best performance) to maximize charge pump efficiency. Typical values are 1uF for the HPVDD, HPVSS and flying capacitors.

POWER SUPPLY DECOUPLING CAPACITORS

The PAM8908 TureCapFree headphone amplifier requires adequate power supply decoupling to ensure that output noise and total harmonic distortion (THD) remain low. Use good low equivalent-series-resistance (ESR)
ceramic capacitors (X5R material or better is required for best performance). Place a 2.2uF capacitor within 5 mm of the PVDD pin. Reducing the distance between the decoupling capacitor and PVDD minimizes parasitic inductance and resistance, improving PAM8908 supply rejection performance. Use 0402 or smaller size capacitors if possible.

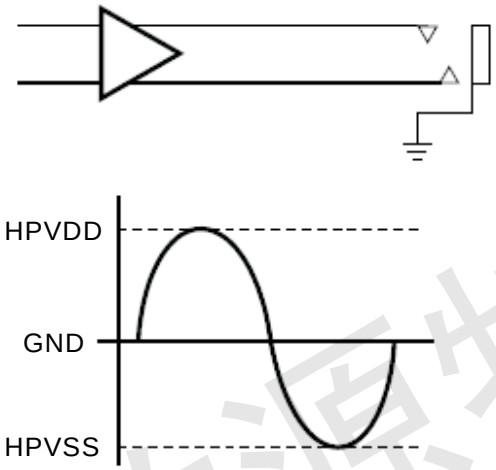
POWER SUPPLY SEQUENCING

Use input coupling capacitors to ensure inaudible turn-on pop. Activate the PAM8908 after all audio sources have been activated and their output voltages have settled. On power-down, deactivate the PAM8908 before deactivating the audio input source. The EN pin controls device shutdown: Set to 0.6 V or lower to deactivate the PAM8908; set to 1.4 V or higher to activate.

Application Information

TRUECAPFREE HEADPHONE AMPLIFIERS

The TrueCapFree amplifier architecture operates from a single supply voltage and uses two internal charge pumps to generate a positive supply and a negative supply rail for the headphone amplifier. The output voltages are centered around 0 V and are capable of positive and negative voltage swings as shown in the following drawing.



TrueCapFree amplifiers require no output dc-blocking capacitors. The headphone connector shield pin connects to ground and will interface with headphones and non-headphone accessories. The PAM8908 is a TrueCapFree amplifier.

LAYOUT RECOMMENDATIONS

EXPOSED PAD ON PAM8908JR

Solder the exposed metal pad on the PAM8908 TQFN package to the landing pad on the PCB. Connect the landing pad to ground or leave it electrically unconnected(floating). Do not connect the landing pad to PVDD or to any other power supply voltage.If the pad is grounded, it must be connected to the same ground as the PGND pin 9. Soldering the thermal pad is required for mechanical reliability and enhances thermal conductivity of the package.

GND CONNECTIONS

The SGND pin is an input reference and must be connected to the headphone ground connector pin. This ensures no turn-on pop and minimizes output offset voltage. Do not connect more than ±0.3 V to SGND.
PGND is a power ground. Connect supply decoupling capacitors for PVDD, HPVDD, and HPVSS to PGND.

POWER SUPPLY CONNECTIONS

Connect the supply voltage to the PVDD pin and decouple it with an X5R or better capacitor. Place both PVDD capacitor within 5 mm of PVDD pin on the PAM8908. Ensure that the ground connection of PVDD capacitor has a minimum length return path to the device. Failure to properly decouple the PAM8908 may degrade audio or EMC performance.

Ordering Information

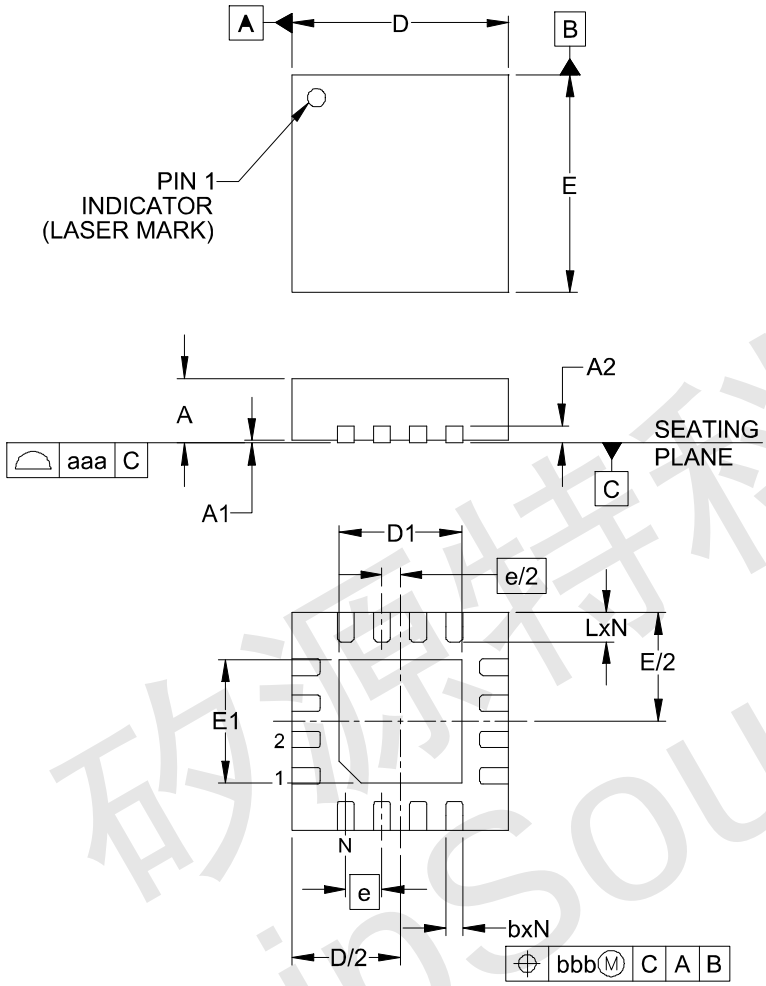
PAM8908 X X X

- X: Shipping Package
- X: Pin Assignment
- X: Package Type

Part Number	Package Type	Shipping Package
PAM8908JER	TQFN3X3-16L	3,000 Units/ Tape & Reel

Outline Dimensions

3x3 mm TQFN 16



DIMENSIONS (Millieters)			
	MIN	TYP	MAX
A	0.40	0.50	0.60
A1	0.00	0.02	0.05
A2		0.20	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
D1	1.55	1.70	1.80
E	2.90	3.00	3.10
E1	1.55	1.70	1.80
e		0.50BSC	
L	0.30	0.40	0.50
N		16	
aaa		0.08	
bbb		0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP IS 1.90 x 1.90mm.